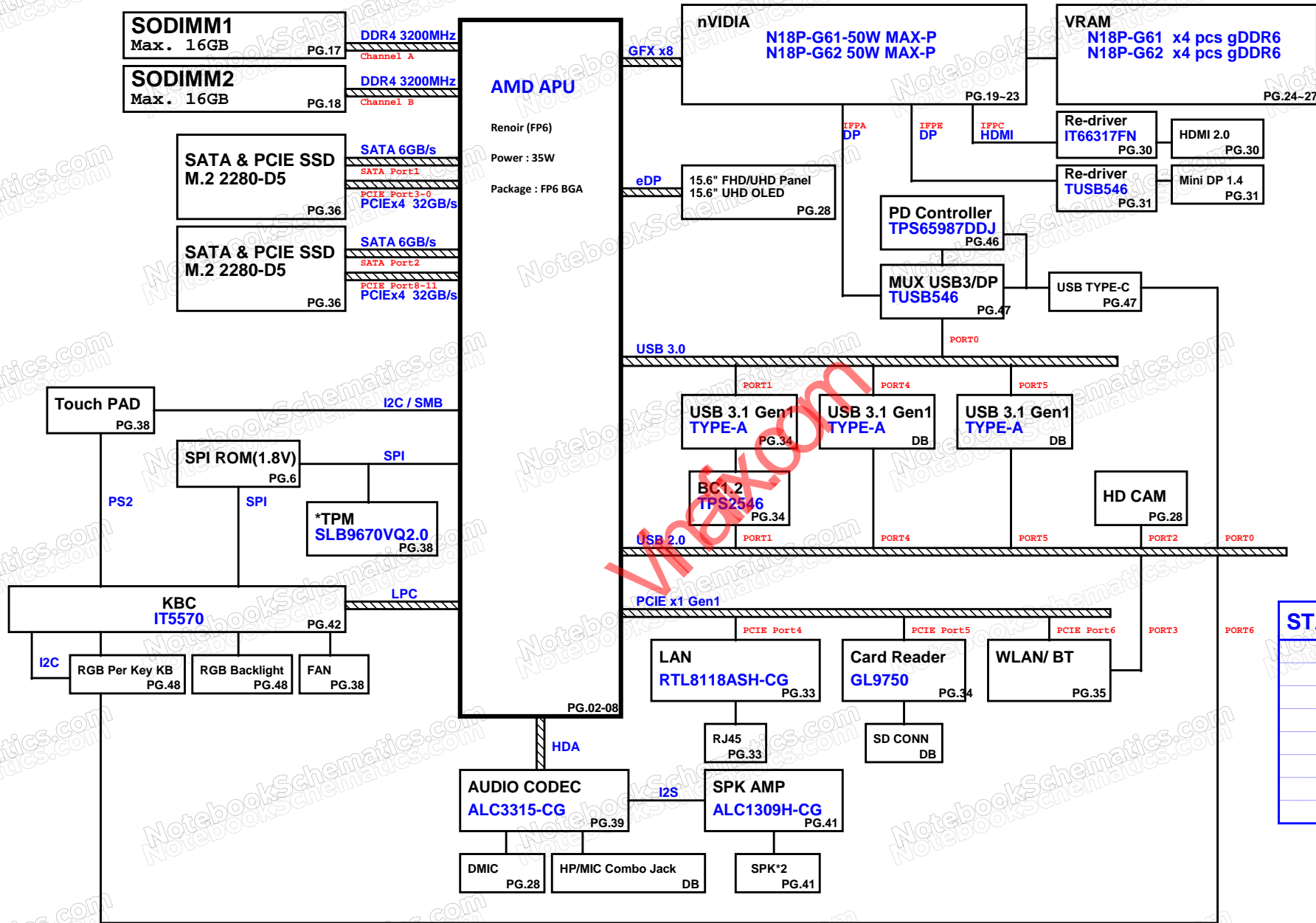


Valkyrie AMD Renoir & NV N18P G61/G62



STACKUP

TOP
GND
IN1
IN2
VCC
IN3
GND
BOT



PROJECT : G3ED
Quanta Computer Inc.

Size: Custom
Document Number: **Starmade Block Diagram**
Date: Tuesday, April 07, 2020
Sheet: 1 of 106
Rev: 1A

PCIe Port	Function
GFX 0~8	GPU
PCIe 3~0	SSD1(PCIe/SATA)
PCIe 4	LAN
PCIe 5	WLAN
PCIe 6	CARD Reader
PCIe 7	NC
PCIe 8~11	SSD2(PCIe/SATA)

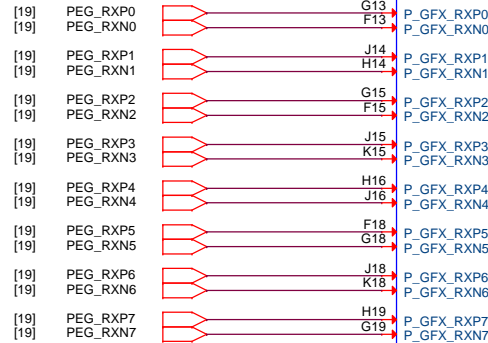
PCIe-SSD 4 lane
(Port3 --> Port0)

LAN

CARD

WLAN

PCIe-SSD 4 lane
(Port8 --> Port11)



SSD SATA/PCIe exchange port

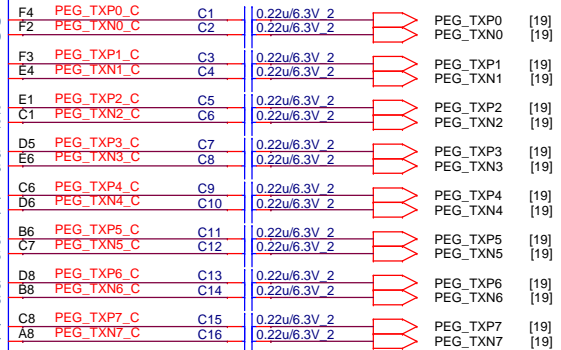
SSD SATA/PCIe exchange port

PCIe

FP6 REV 0.92
PART 2 OF 13

*CPU_AMD_FP6

AMD APU	TOPBSQ PN	Quanta PN	Stage
R9-4900U 2.0G	NA	AJ00100UT00	DB



SSD SATA/PCIe exchange port

SSD SATA/PCIe exchange port

PCIe-SSD 4 lane
(Port3 --> Port0)

LAN

CARD

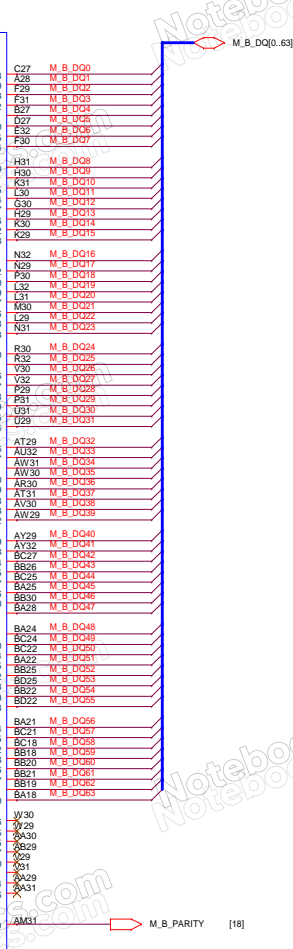
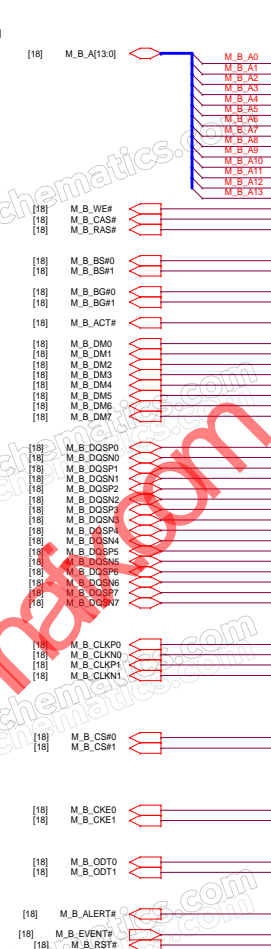
WLAN

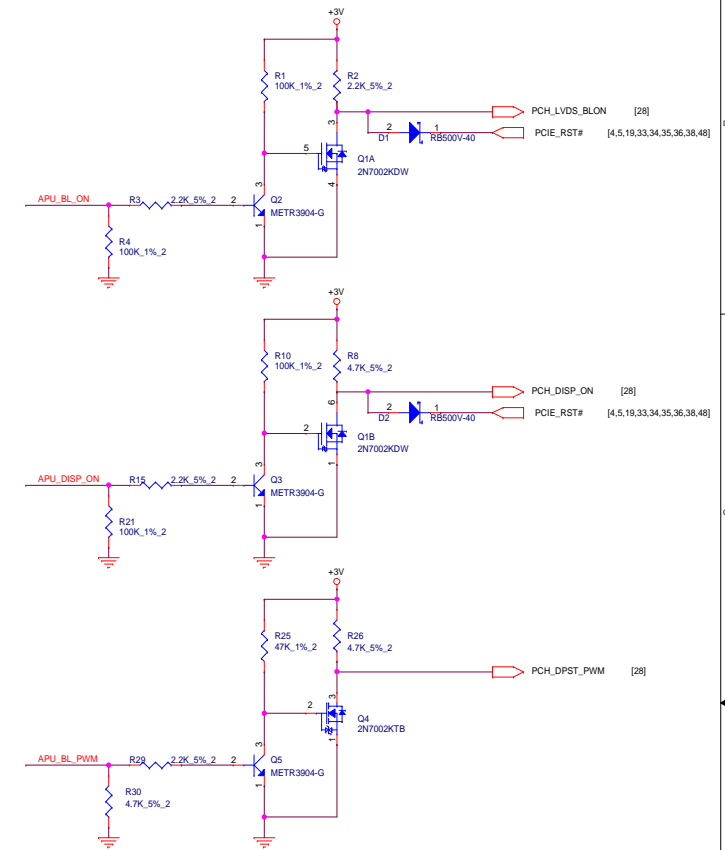
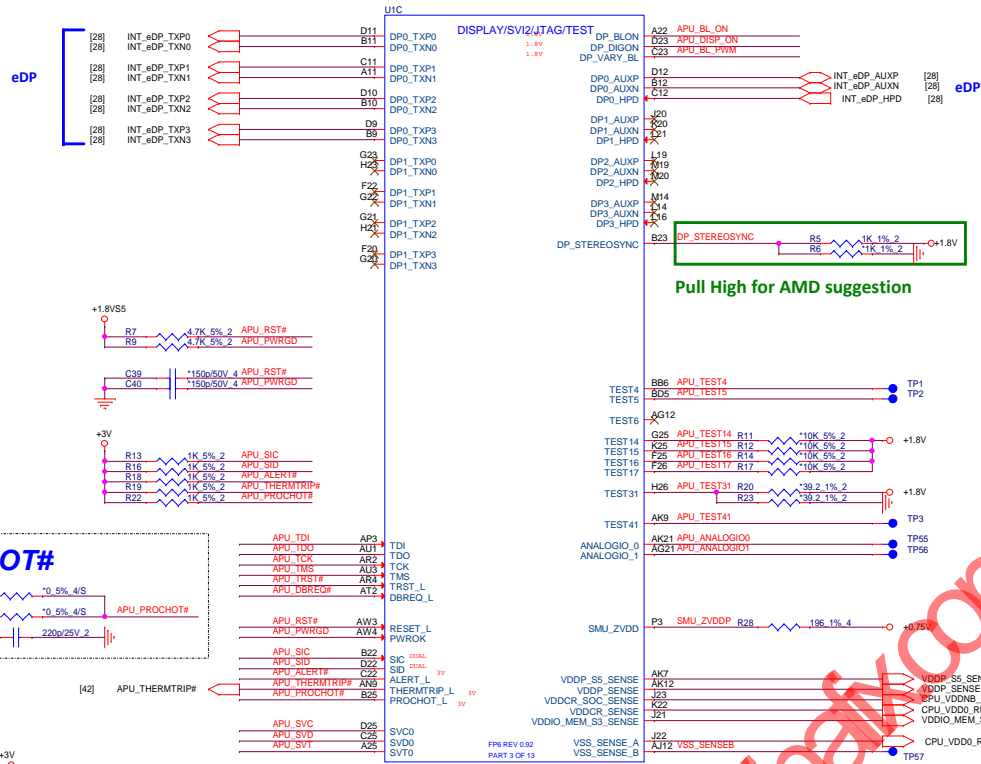
PCIe-SSD 4 lane
(Port8 --> Port11)



PROJECT : Valkyrie
Quanta Computer Inc.

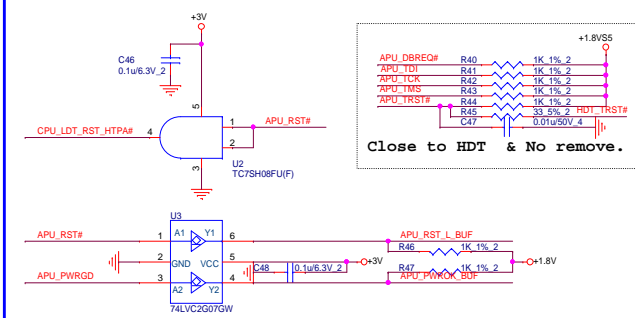
Size	Document Number	Rev
Custom	RENOIR 1/7(PCIe)	1A
Date: Tuesday, April 07, 2020	Sheet 2 of 106	





HDT+ Connector for Debug only

Can remove on MP



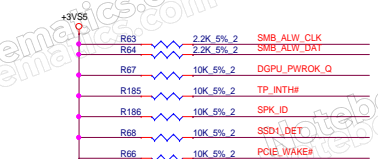
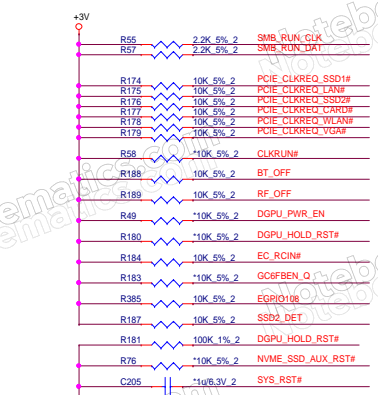
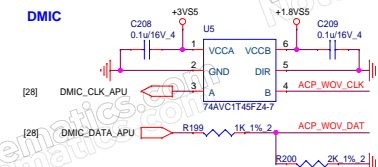
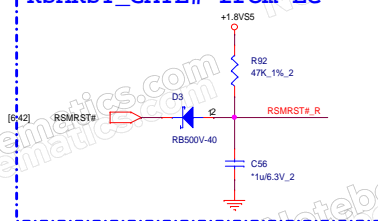
PN	
EU (V1)	DFFC20FR255
EP (V1)	DFFC20FR031



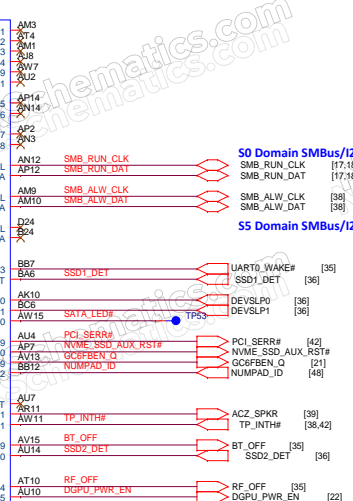
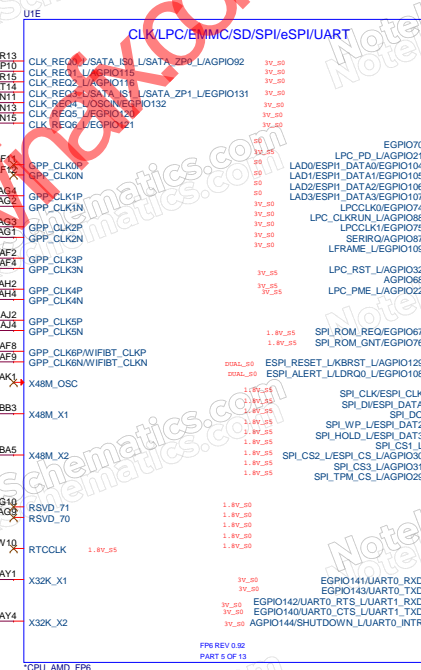
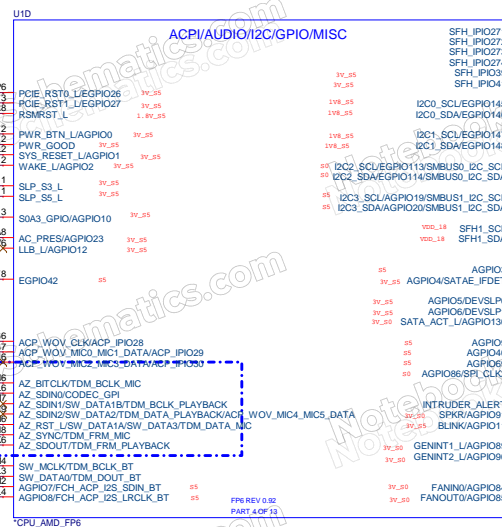
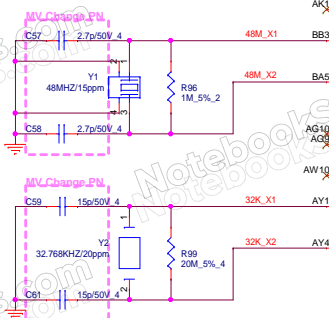
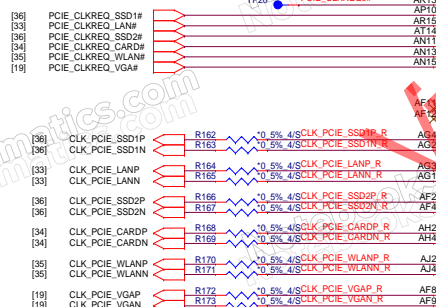
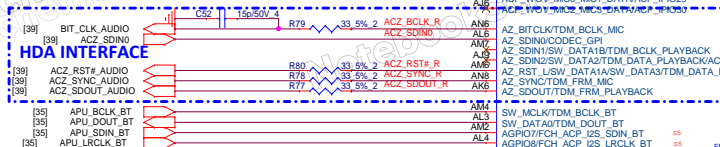
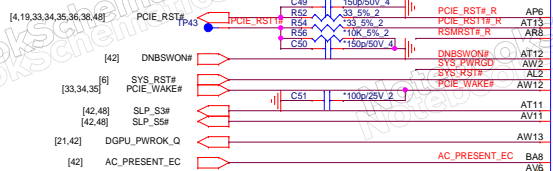
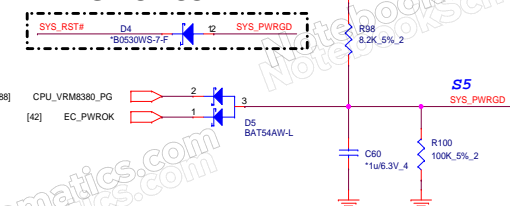
PROJECT : Valkyrie
Quanta Computer Inc.

Size Custom
Document Number
RENOIR 37(DIS/MISC)
Date: Tuesday, April 07, 2020
Sheet 4 of 106

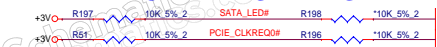
Rev 1A



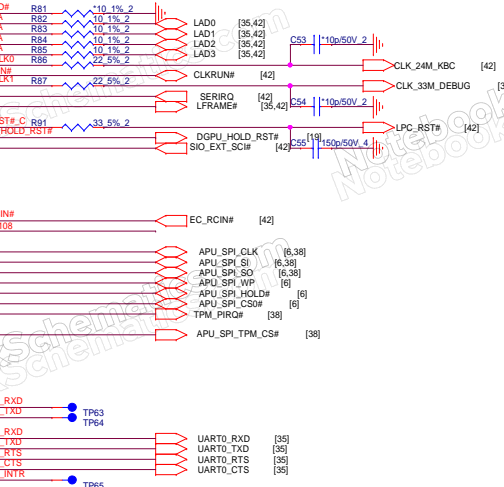
PWRGD CIRCUIT

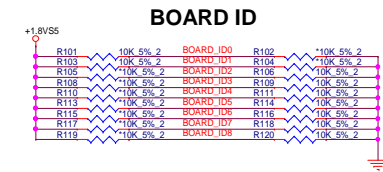


BOARD ID SETTING

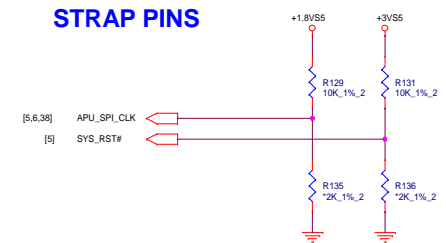


PCIE_CLKREQ0#	SATA_LED#	Definition
0	0	NEW GPU
0	1	N18E-G0
1	0	Reserved
1	1	N18P-G6





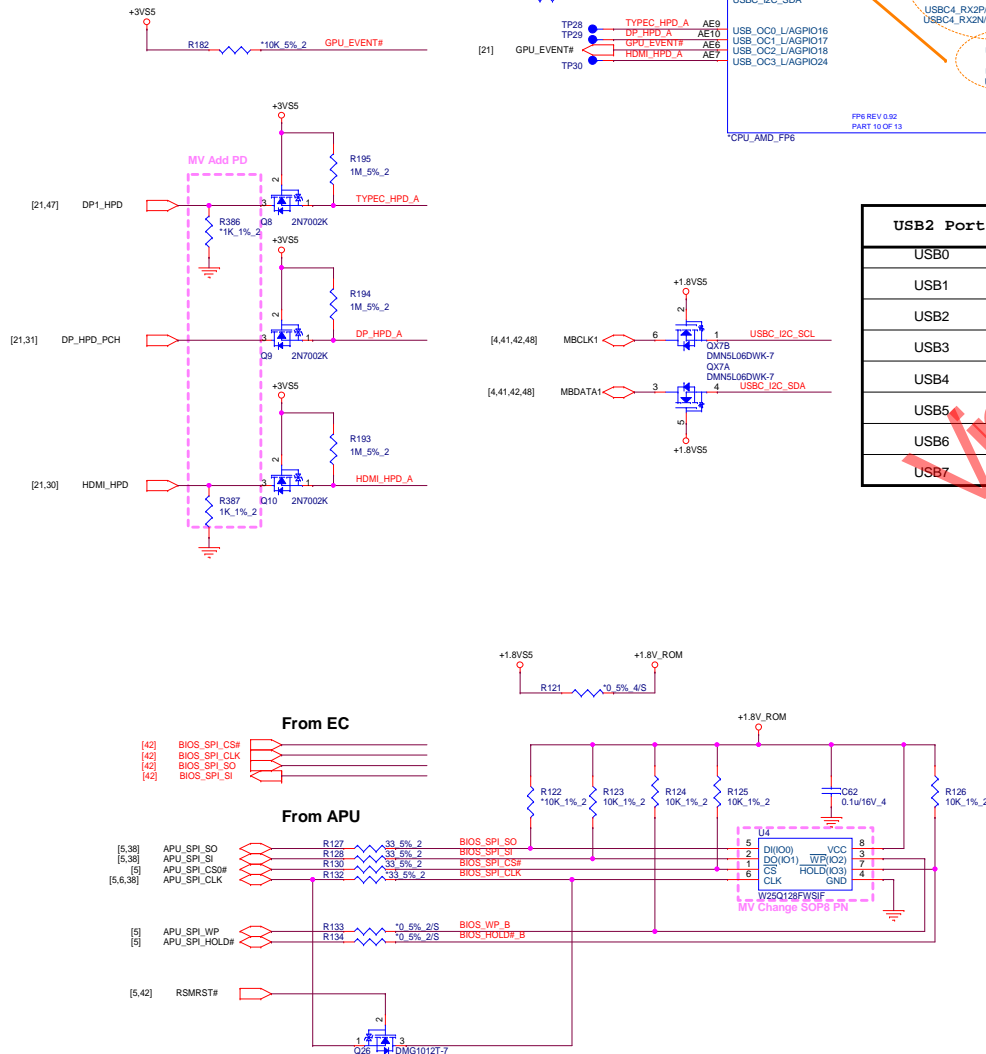
STRAP PINS



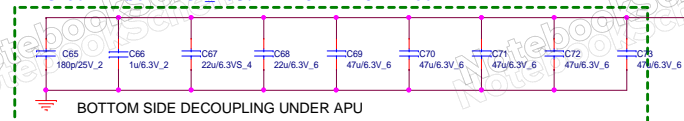
TP31	BIOS_SPI_CS#
TP32	BIOS_SPI_CLK
TP33	BIOS_SPI_SI
TP34	BIOS_SPI_SO
TP35	BIOS_WP_B
TP36	BIOS_HOLD#_B

Vender	Size	P/N (1.8V)
WND	1.6M	AKE5DZNO0N1 W25Q128FWSIF
GGD	1.6M	AKE5DZNO0Q02 GD25LQ128DSIGR
MAX	1.6M	AKE5DZNO0Z00 MX25U12873FM2I-10G
Socket	DG008000011	

Vender	Size	P/N (1.8V)
WND	16M	AKE5DFNKN01 W25Q128FWPIF
GGD	16M	AKE5DZNKQ01 GD25LQ128DWIGF
MAX	16M	AKE5DFNQ05 MX25U12835FZNI-
Socket	DG008000012	

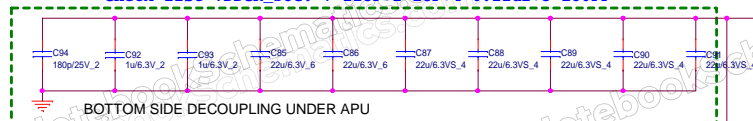


Check list VDDCR SOC: 7*22UF+1*1U+1*180PF

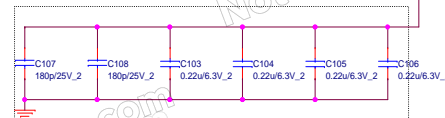


 BOTTOM SIDE DECOUPLING UNDER APU

Check list VDDCR SOC: 7*22UF+2*1UF+4*0.22uf+3*180PF

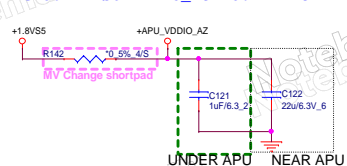


BOTTOM SIDE DECOUPLING UNDER APU



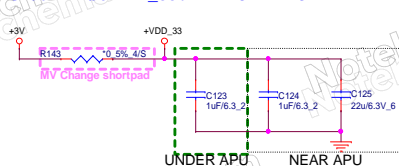
Decoupling between porcess and DIMMs across VDDIO and VSS split.

Check list VDDIO AUDIO: 1*22UF+1*1UF



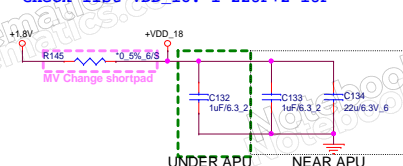
UNDER APU NEAR APU

Check list VDD 33: 1*22UF+2*1UF



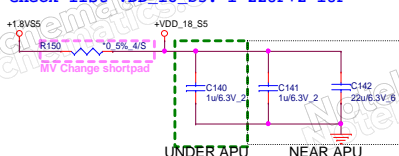
UNDER API NEAR API

Check list VDD 18: 1*22UF+2*1UF



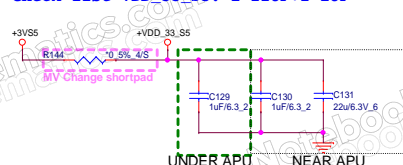
UNDER API NEAR API

Check list VDD 18 S5: 1*22UF+2*1UF

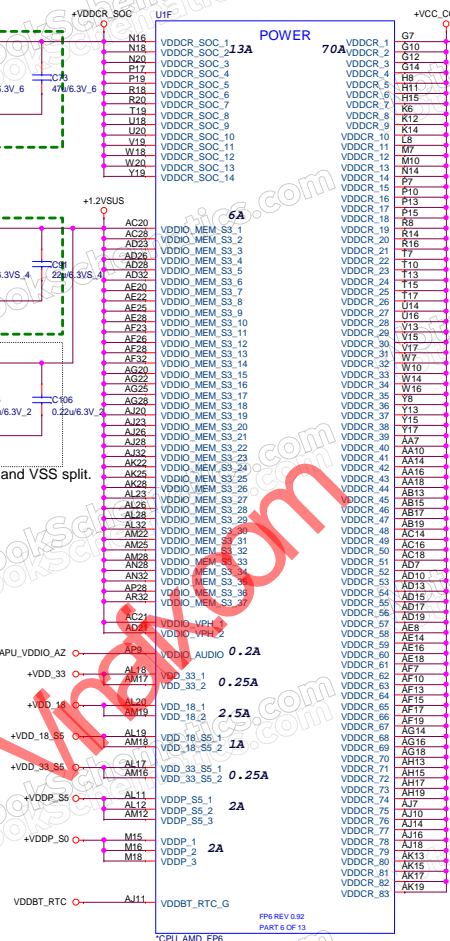


UNDER API

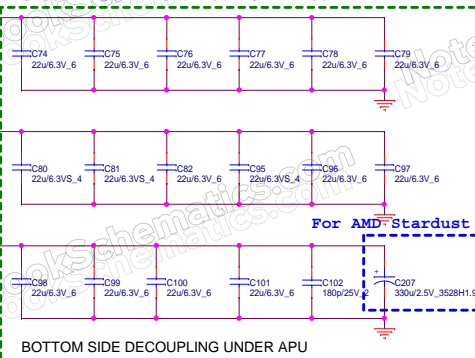
Check list VDD_33_S5: 1*22UF+2*1UF



UNDER APO NEAR APU



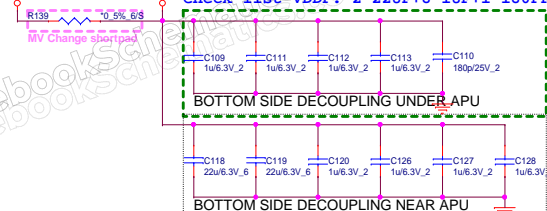
Check list VDDCR: 16*22UF+1*180PF



For AMD Stardust Test

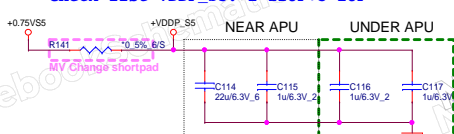
BOTTOM SIDE DECOUPLING UNDER APL

Check list VDDP: 2*22UF+8*1UF+1*180PF

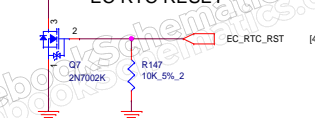


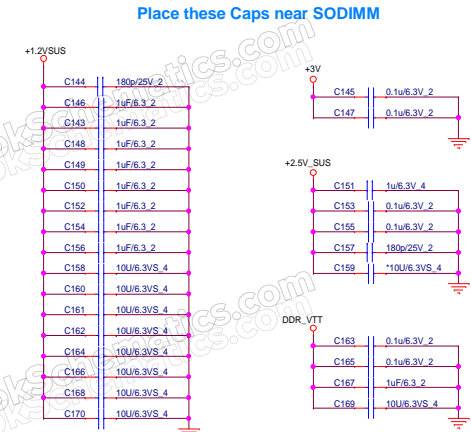
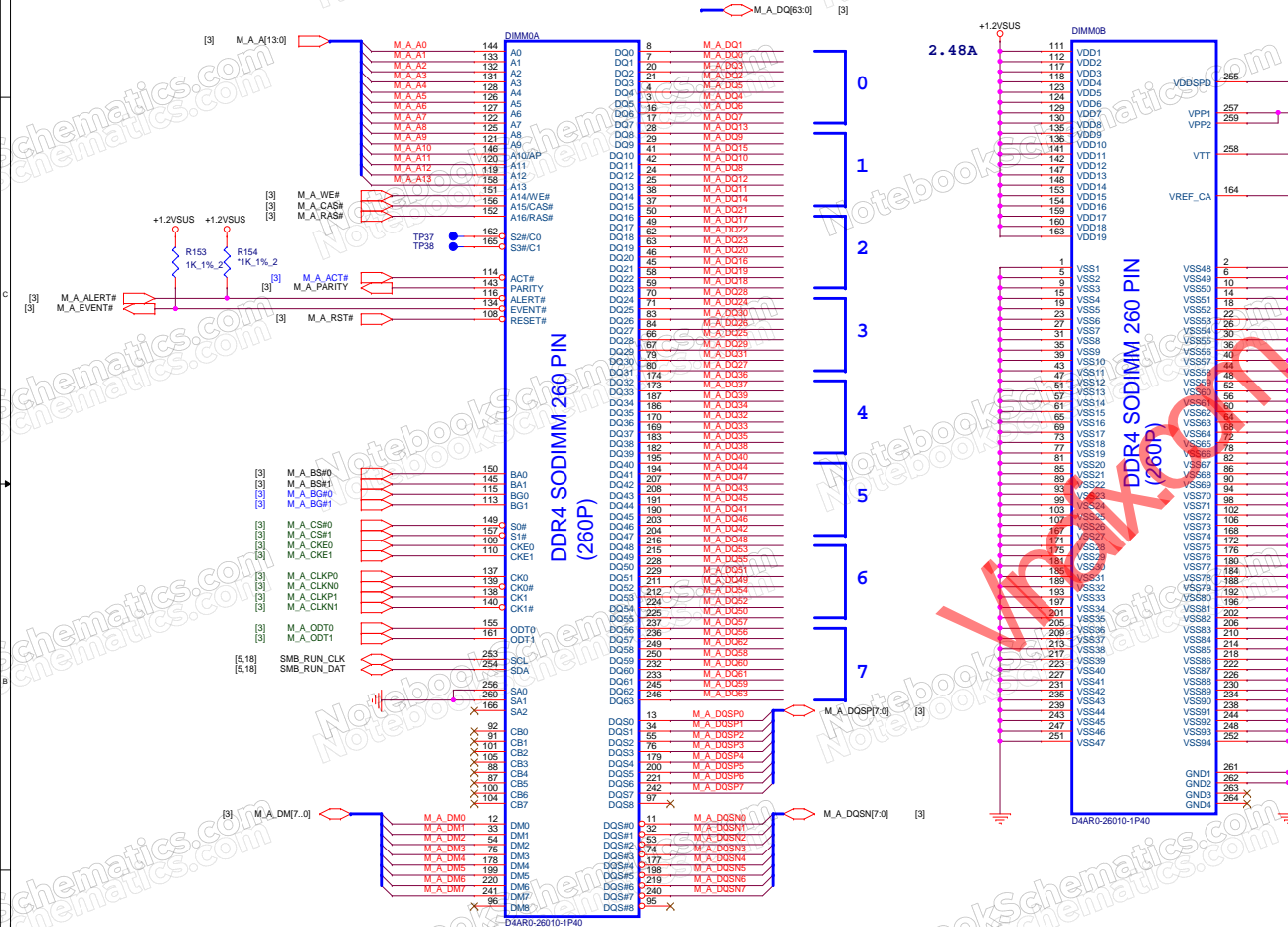
BOTTOM SIDE DECOUPLING NEAR API

Check list VDDP_S5: 1*22UF+3*1UF



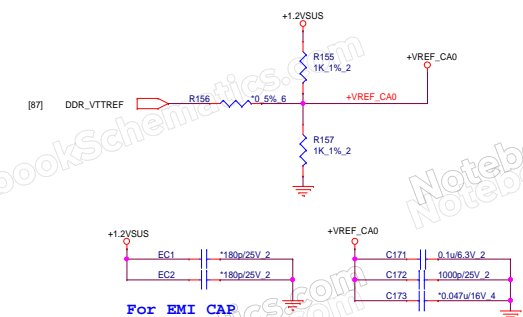
EC RTC RESET



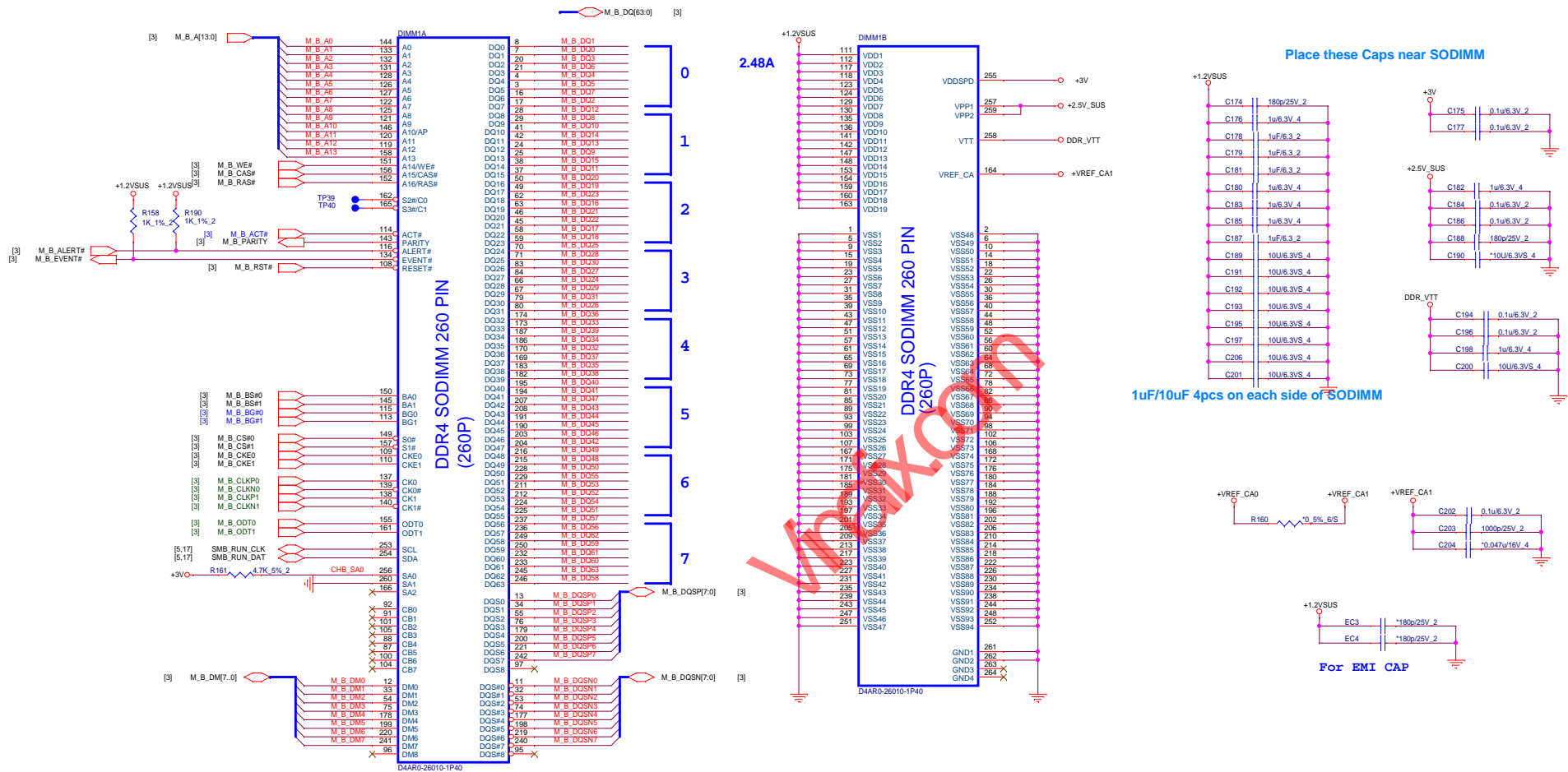


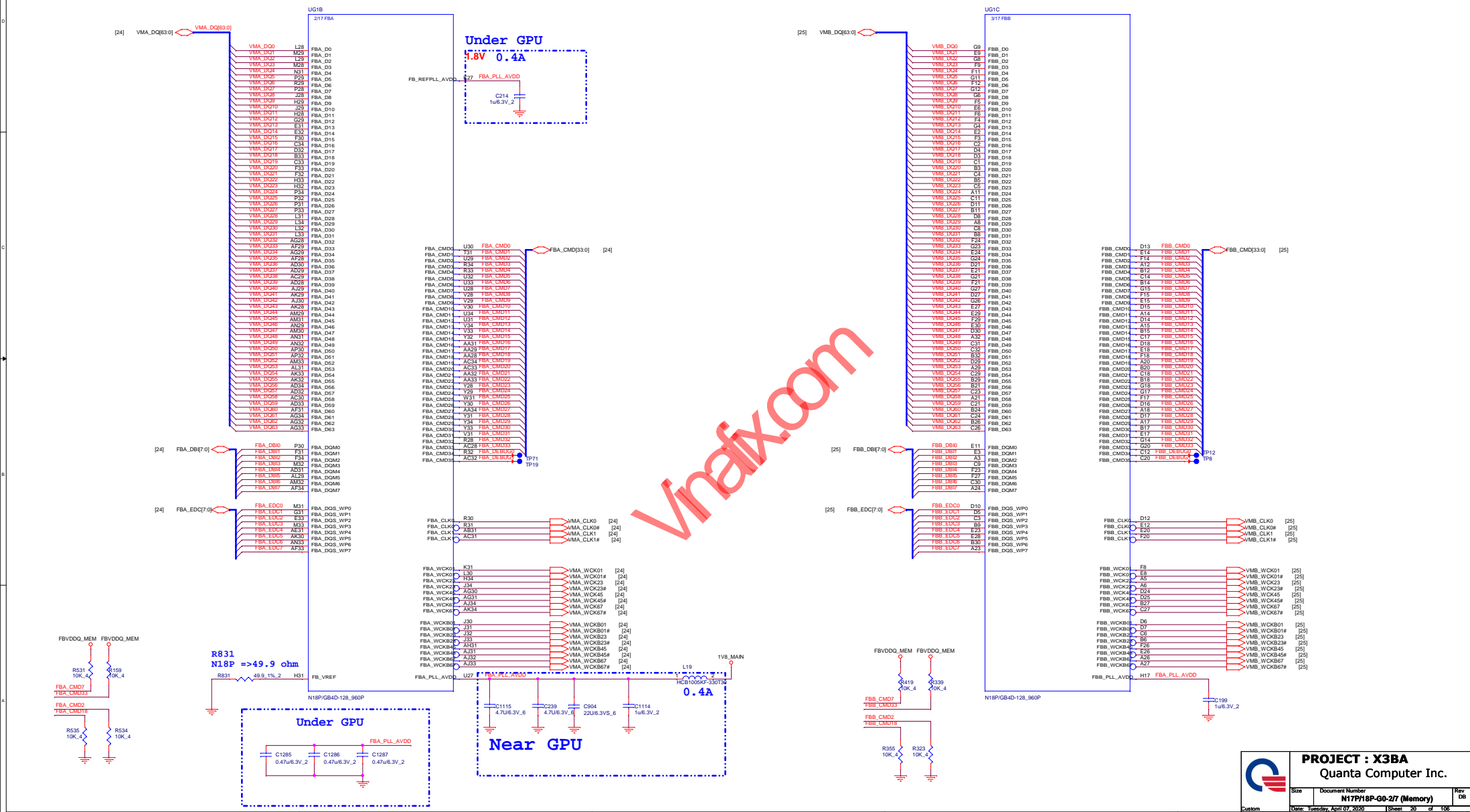
1uF/10uF 4pcs on each side of SODIMM

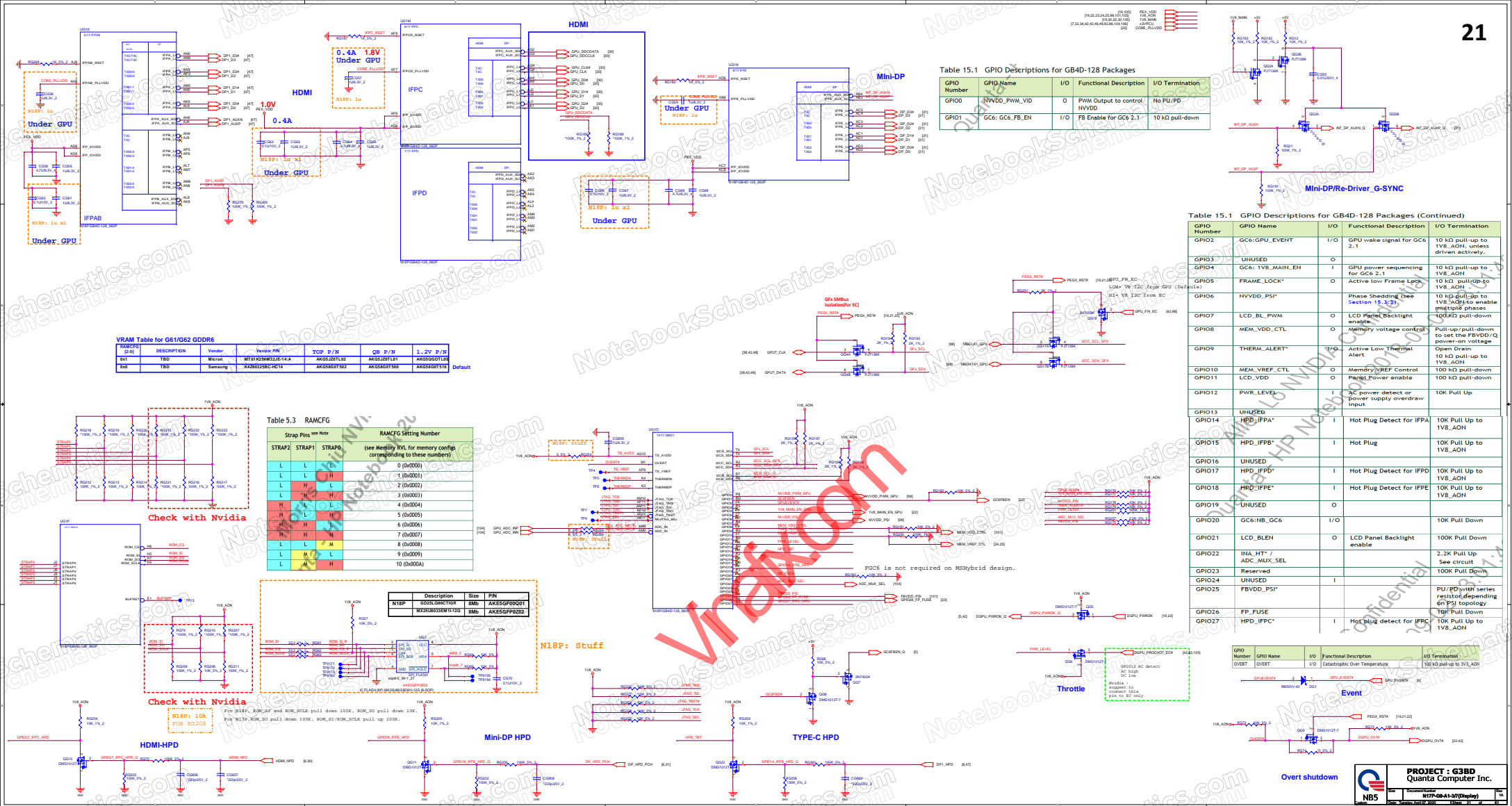
The Celadon CRB change R157 from 1K to 1.5K 1% to workaround DDR issue.

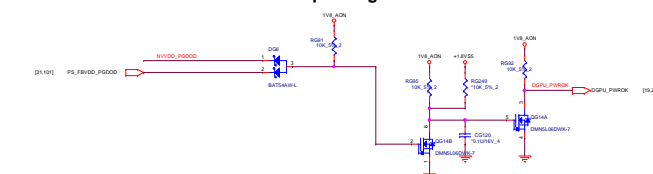
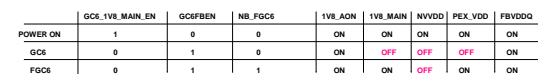
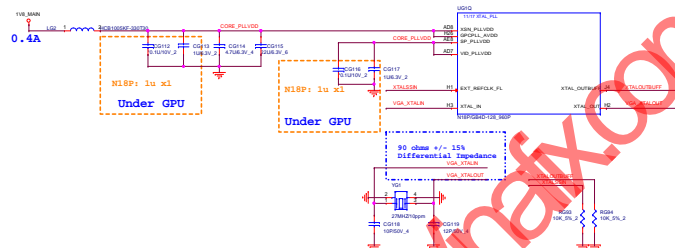
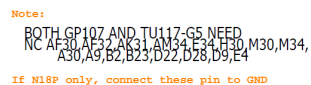


For EMI CAP

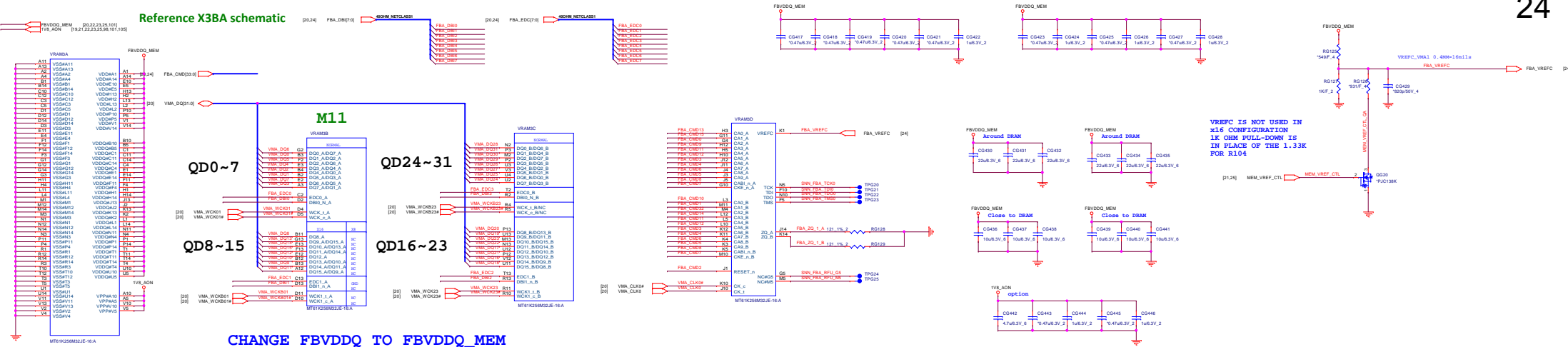




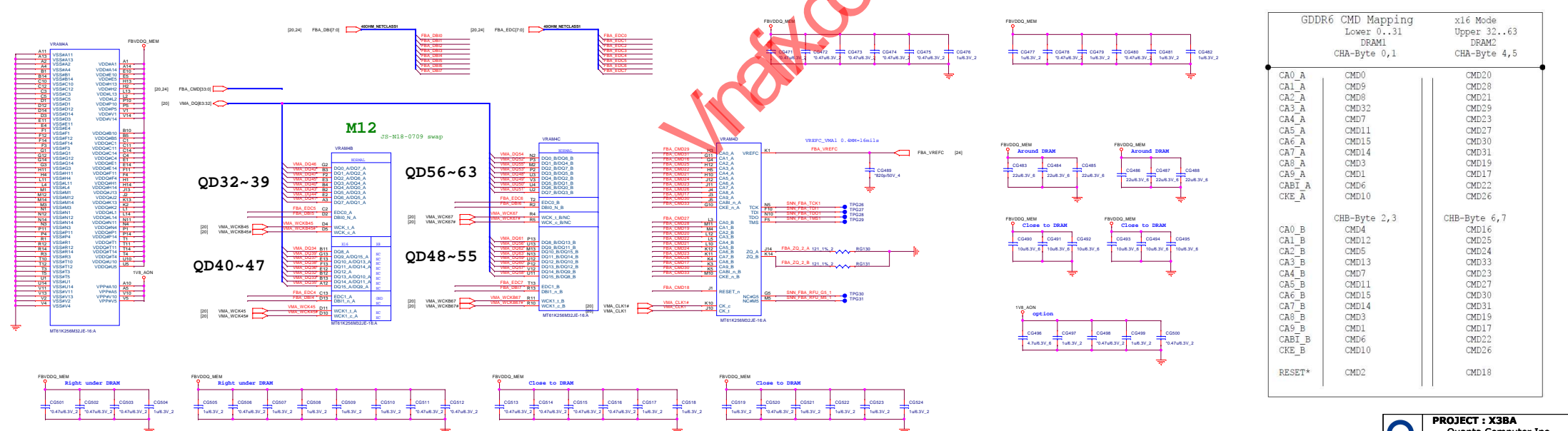




Reference X3BA schematic

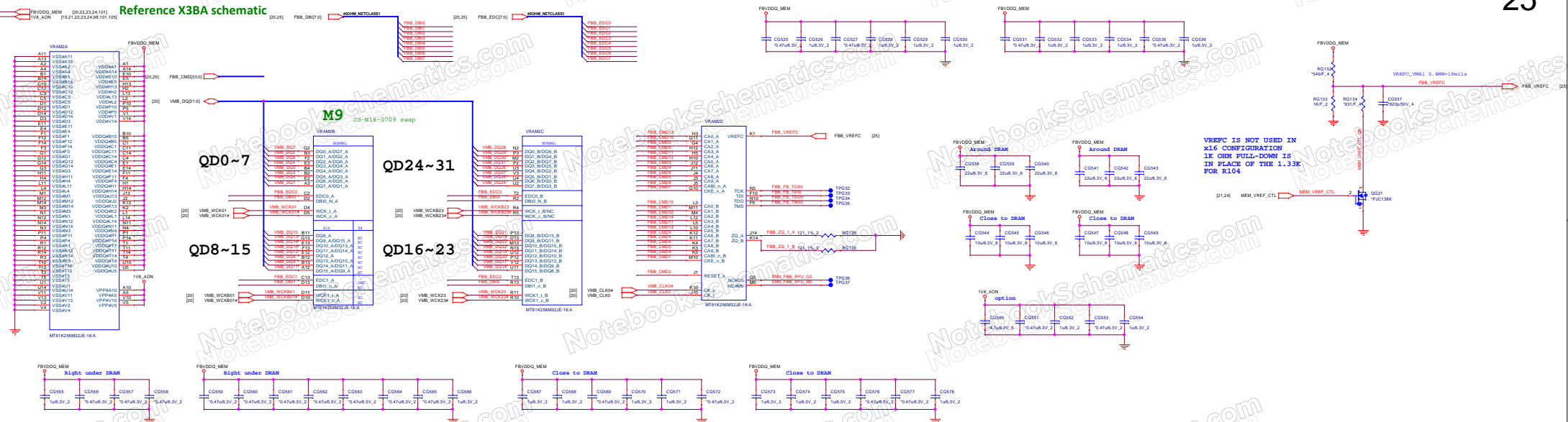


MEMORY: FBA Partition 63..32

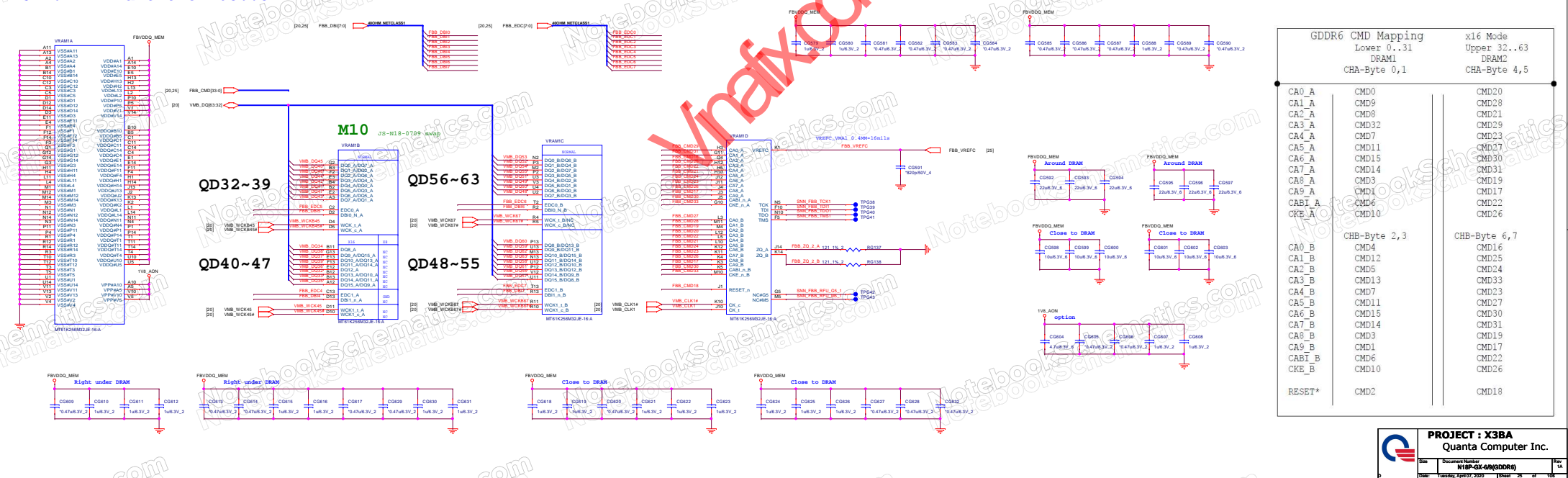


MEMORY: FBB Partition 31..0

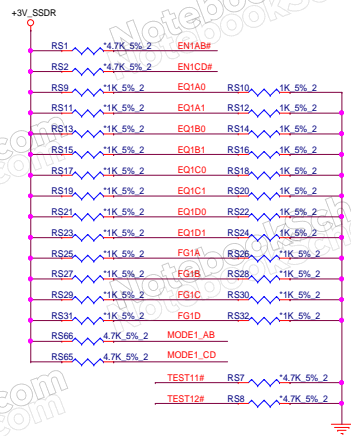
Reference X3BA schematic



MEMORY: FBB Partition 63..32

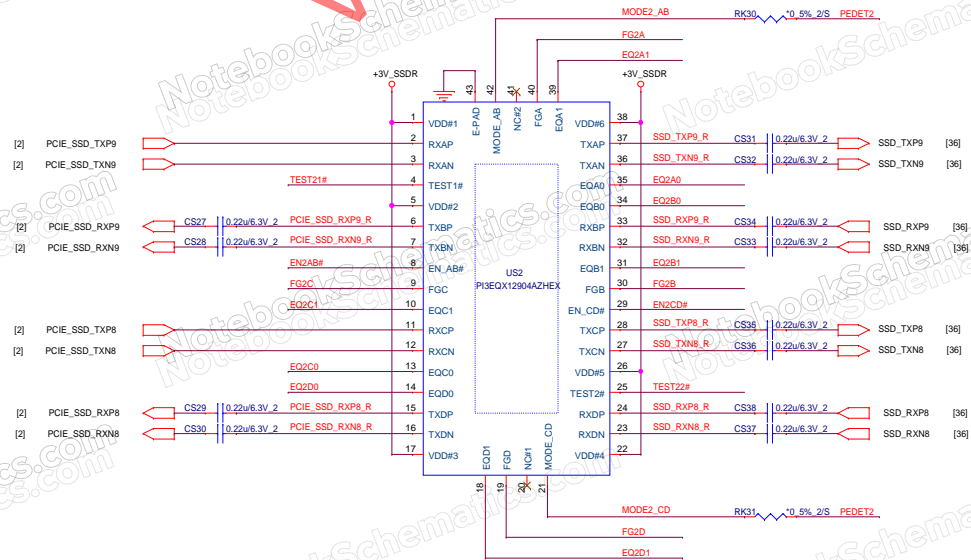
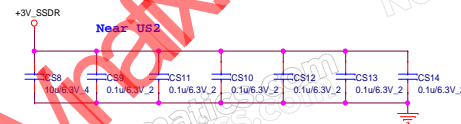
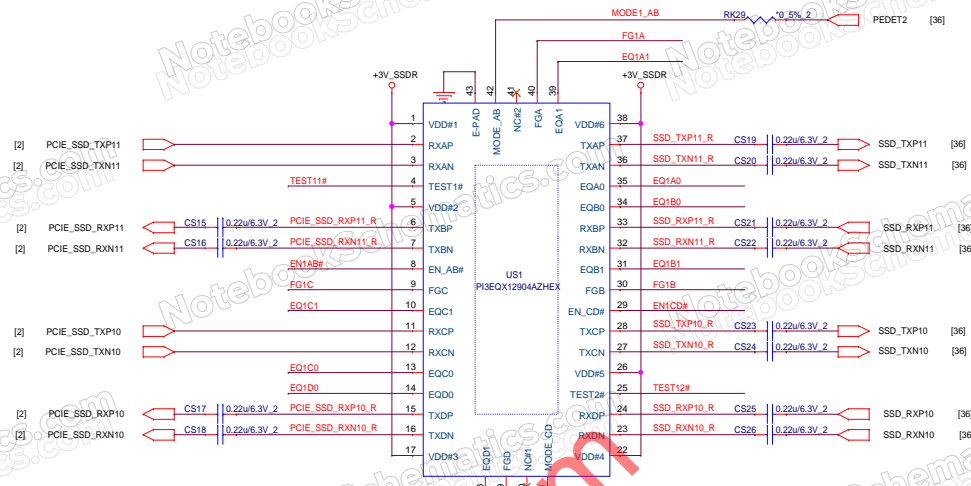
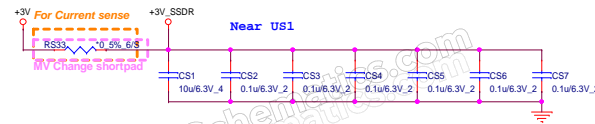
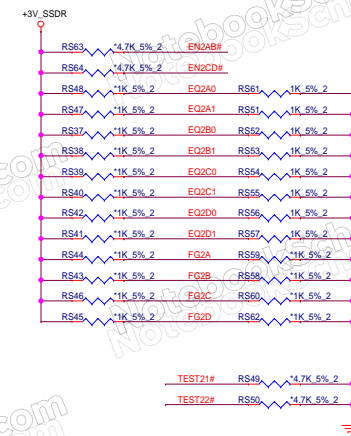


GDDR6 CMD Mapping		x16 Mode
Lower 0..31		Upper 32..63
DRAM1		DRAM2
CHA-Byte 0,1		CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CAB1_A	CMD6	CMD22
CKE_A	CMD10	CMD26
CHB-Byte 2,3		CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CAB1_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

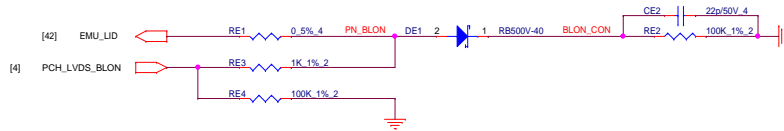


Flat Gain Settings
 0 : -3.5 dB
 R : -1.5 dB
 F : 0 (Default)
 1 : +1.5 dB

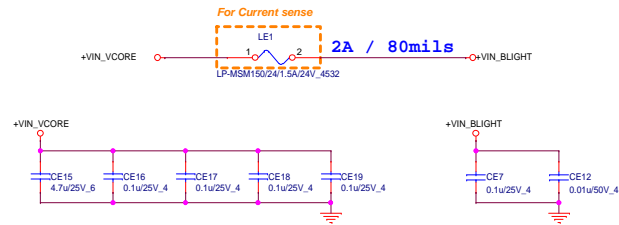
TEST#	MODE (Pin21)	Supported Application
0	X	Active Mode only for any application
1	0	SATA3
1	1	PCIe3



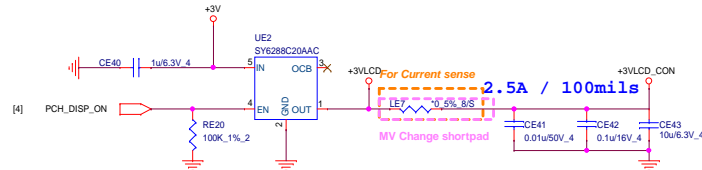
LID Switch



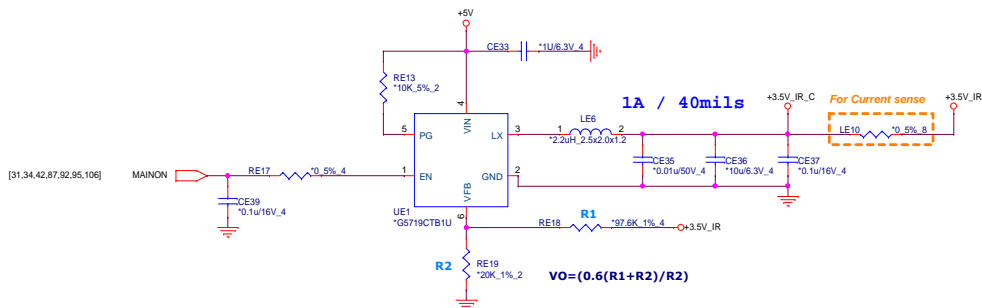
LCD Backlight



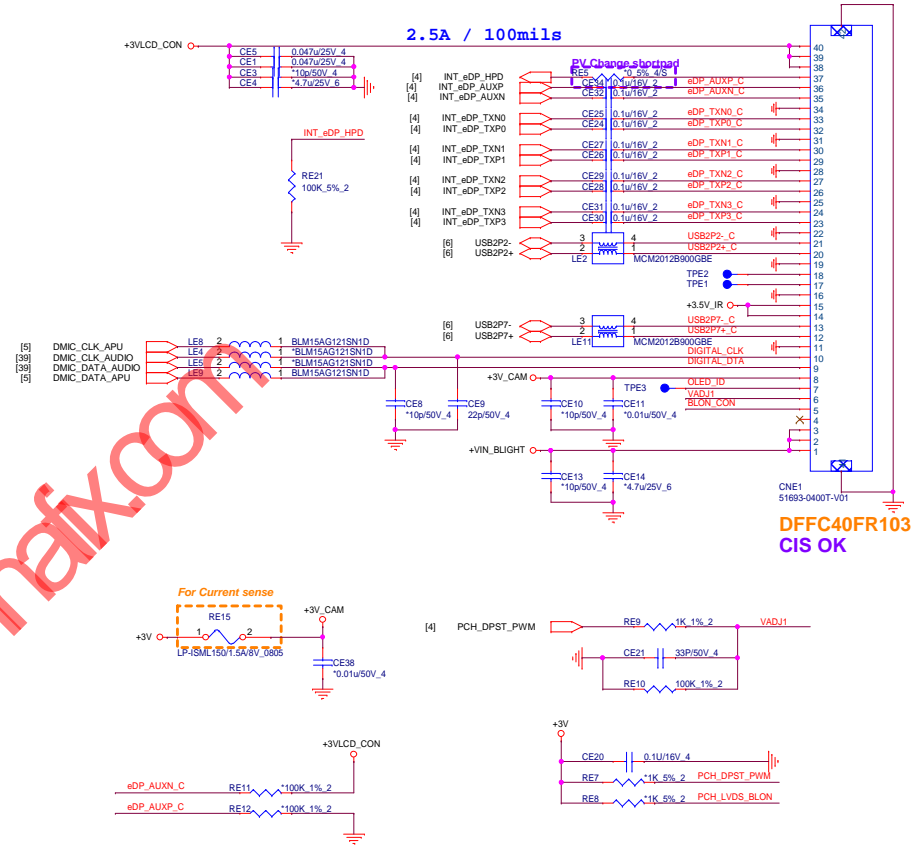
3V LCD Power SW

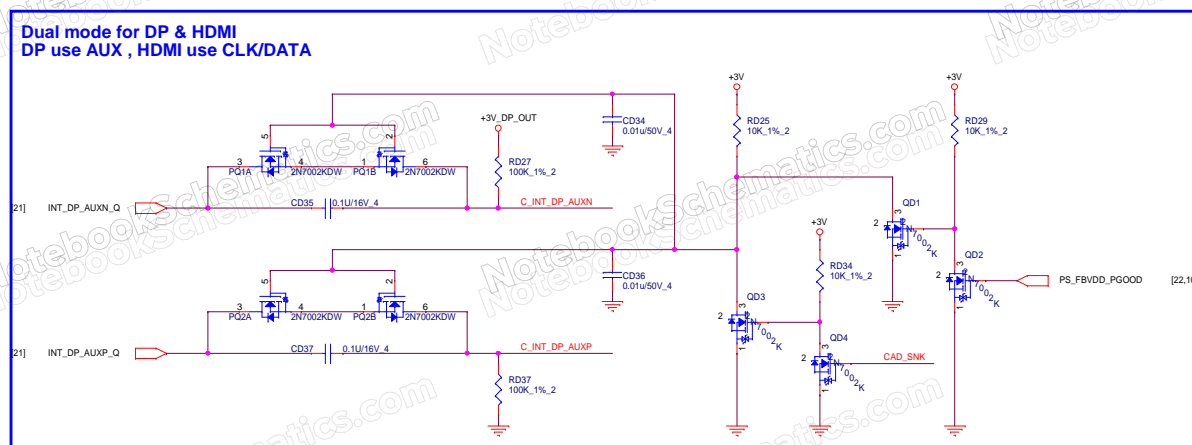
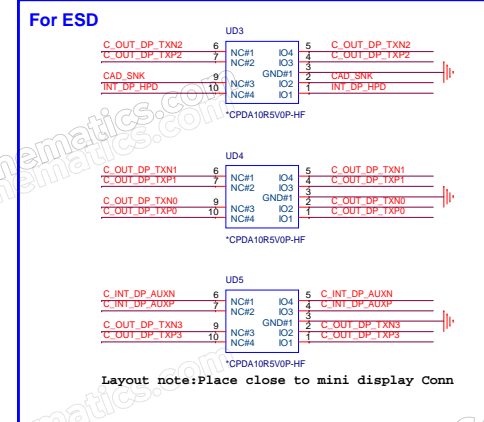


IR CAM Power SW

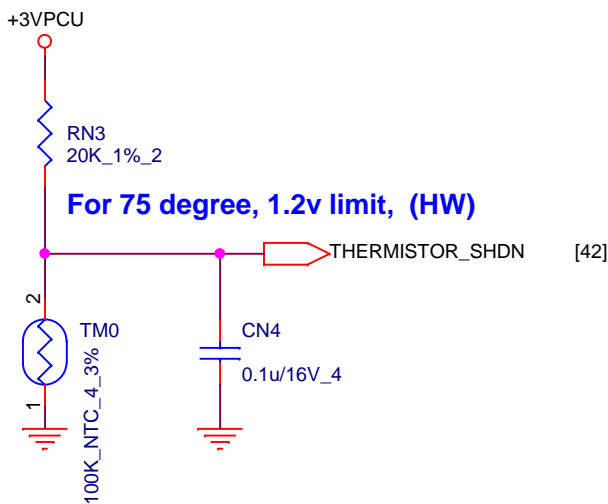


eDP CONN.

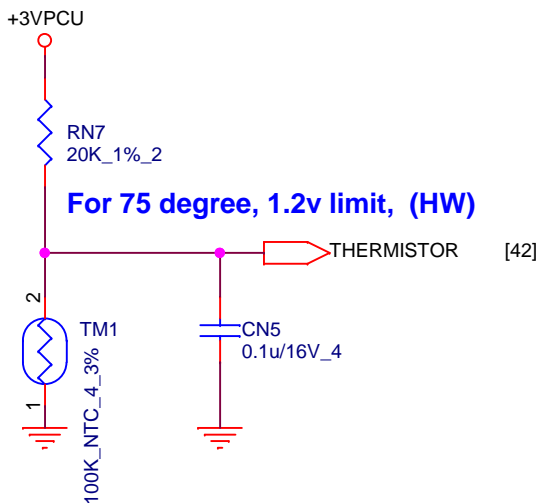




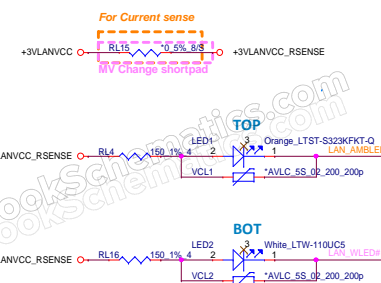
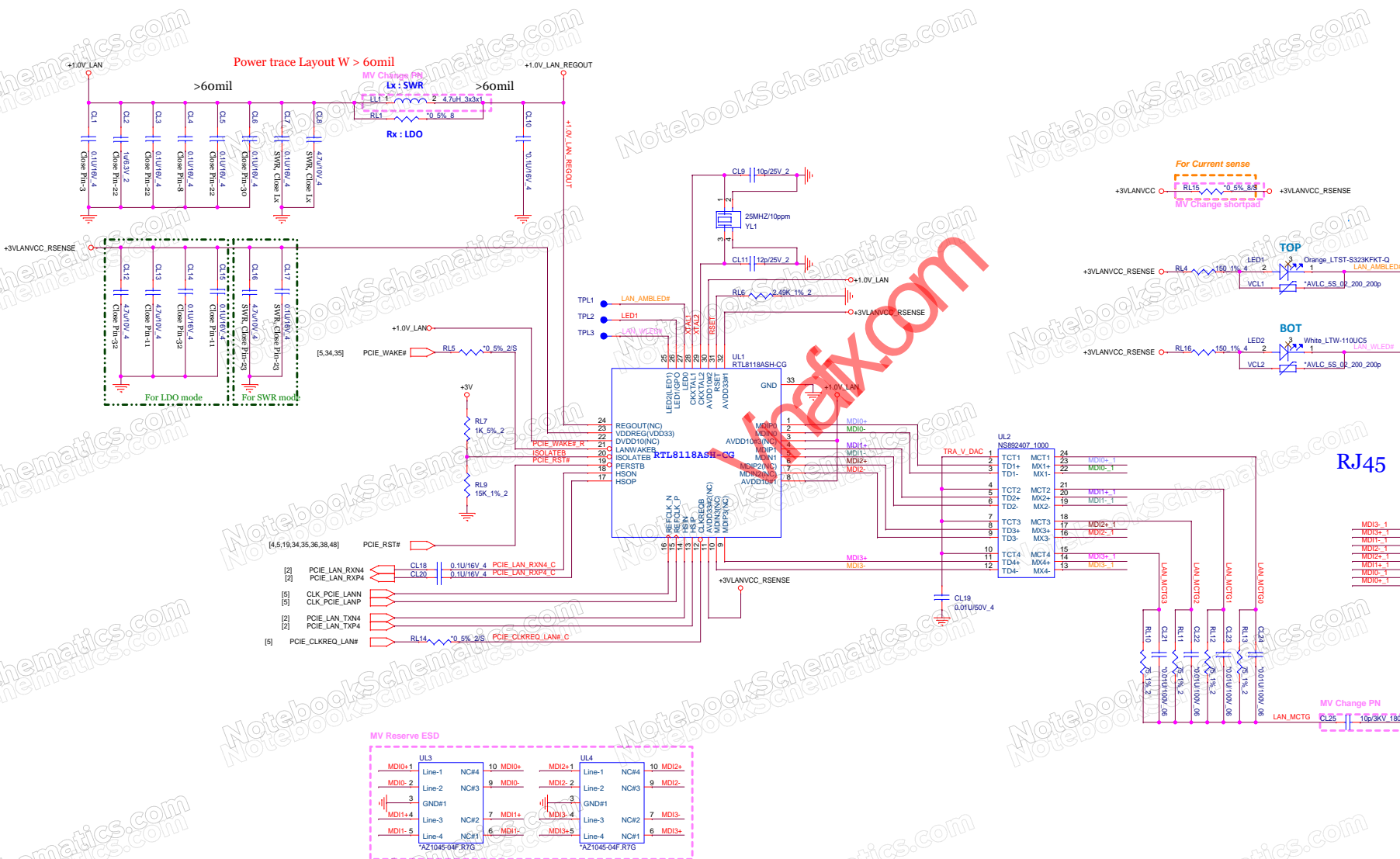
For HW shutdown (TOP nearby CPU)



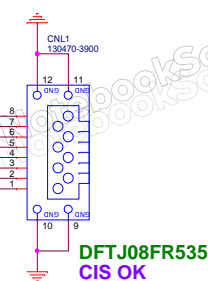
For CPU (Bottom nearby CPU)



LAN & RJ45



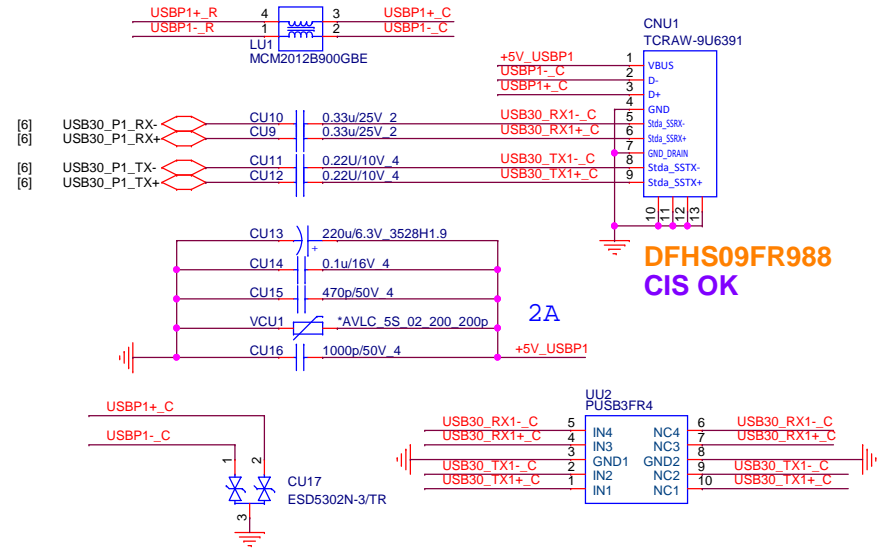
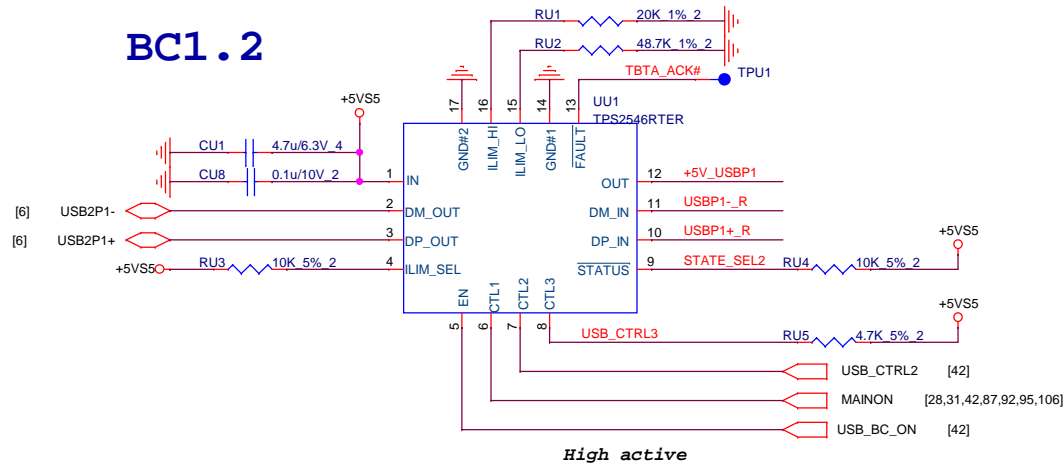
RJ45



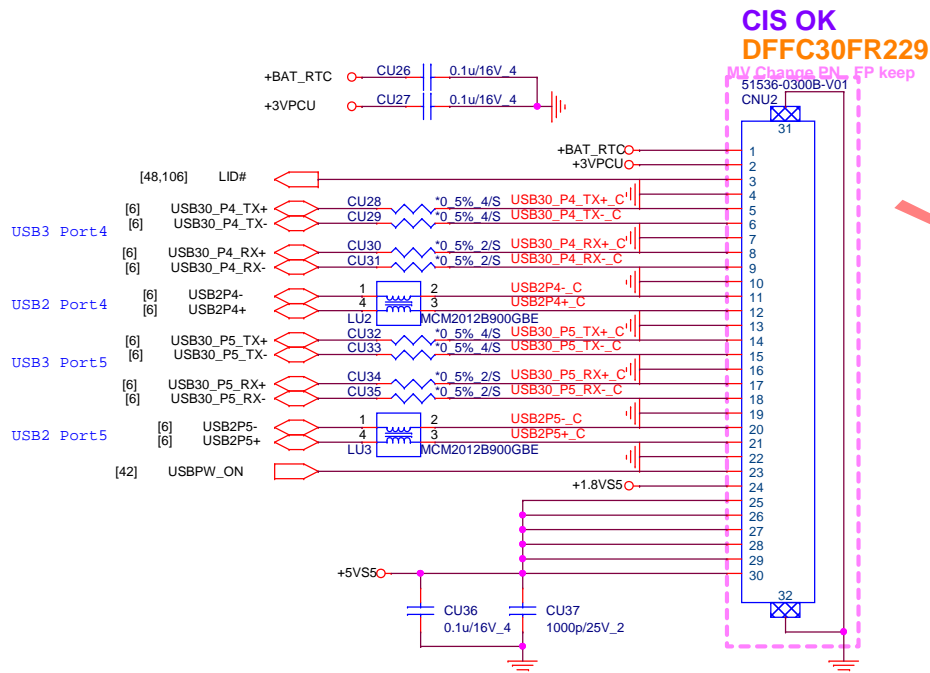
USB 2.0/3.0 Combo MB

34

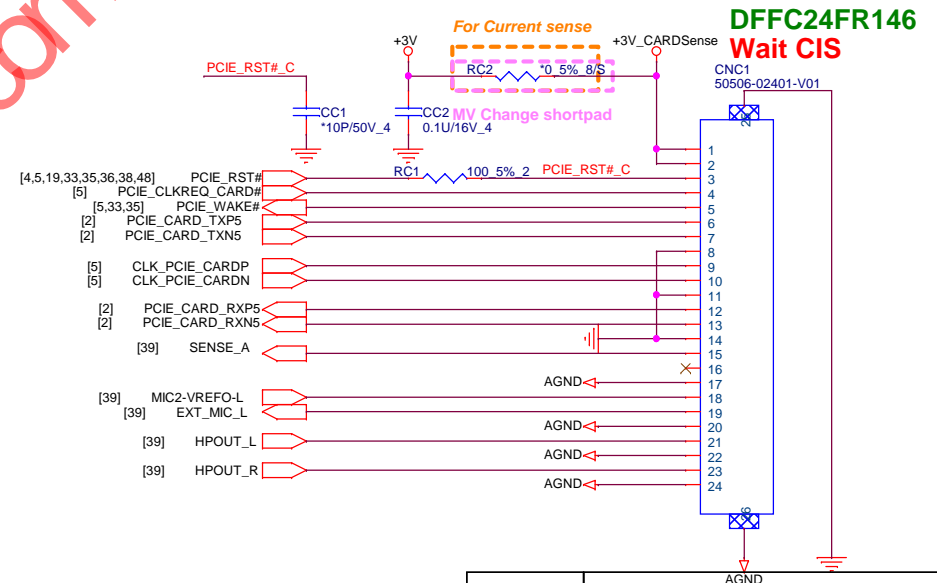
BC1.2



USB small board

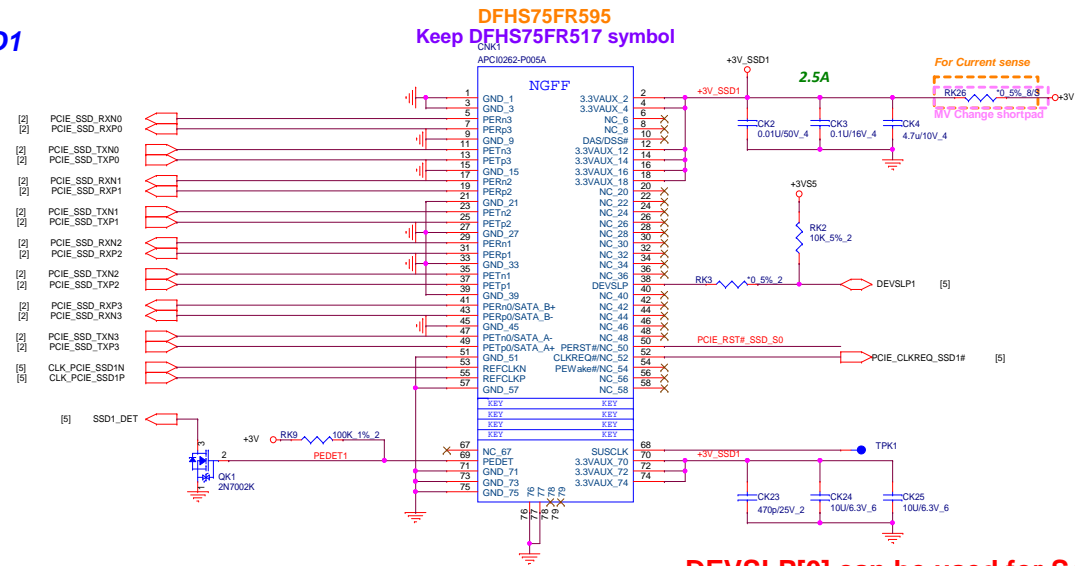


SD Card Audio Jack to Small Board



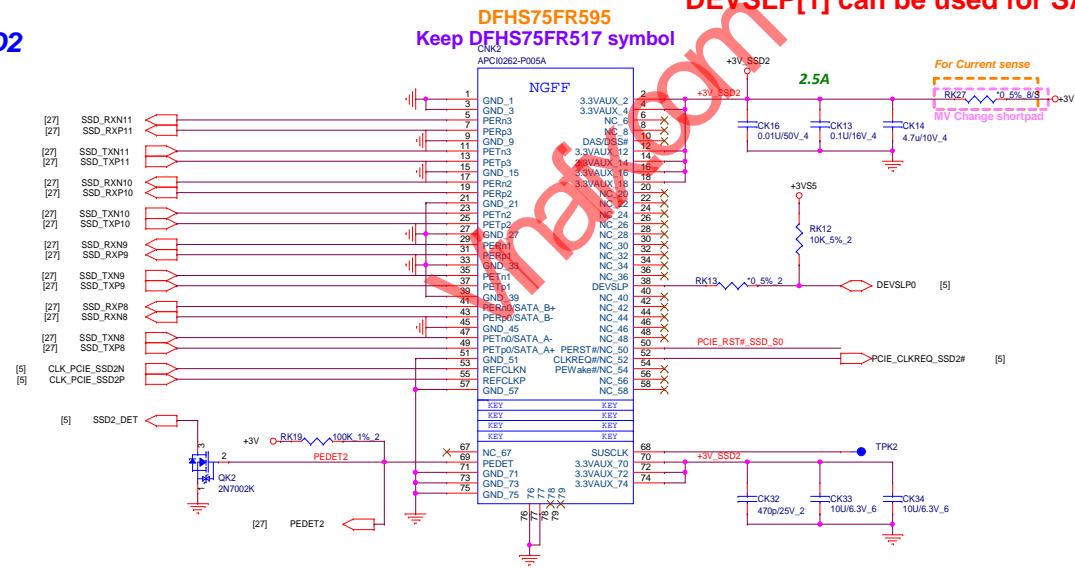
PROJECT : Valkyrie		
Quanta Computer Inc.		
Size	Document Number	Rev
B	USB3.0/SD/USB Small Board	3A
Date: Tuesday, April 07, 2020	Sheet 4	of 106

SSD1

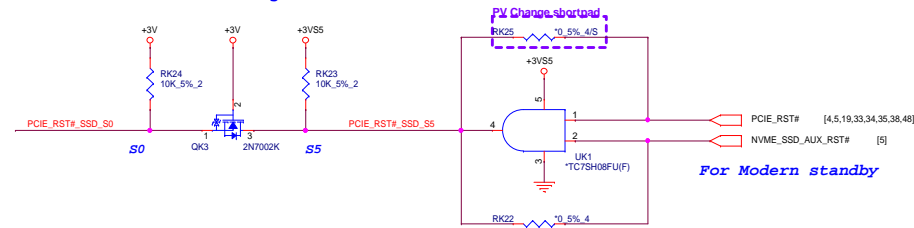


DEVSLP[0] can be used for SATA Port 0 or 2.
DEVSLP[1] can be used for SATA Port 1 or 3

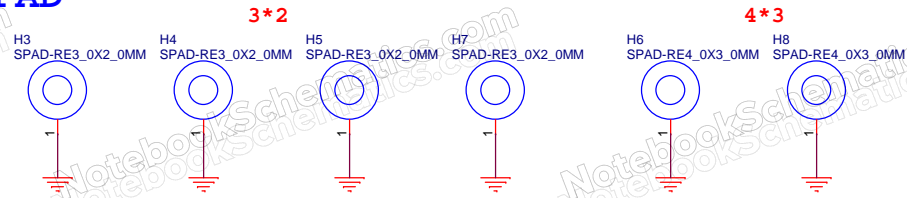
SSD2



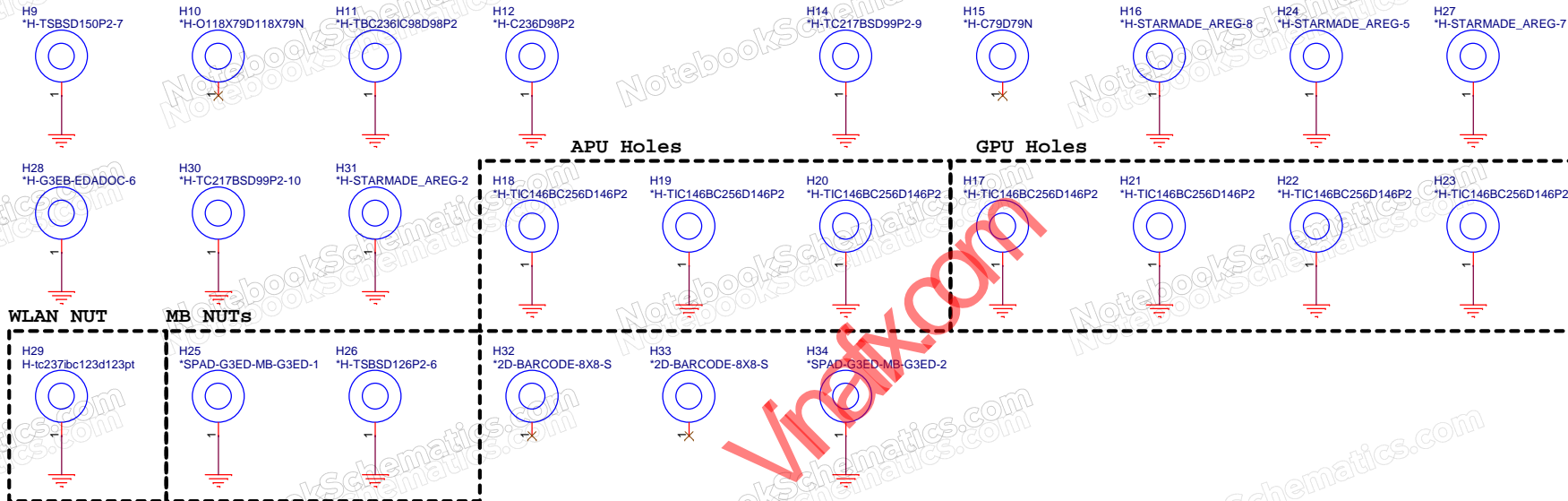
For leakage



EMI PAD

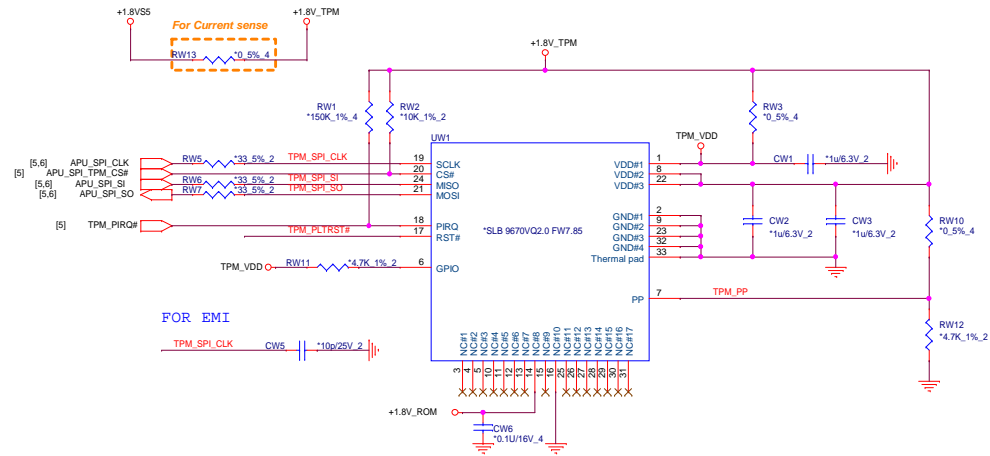
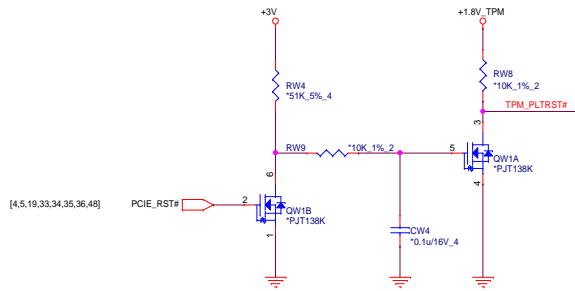


Holes

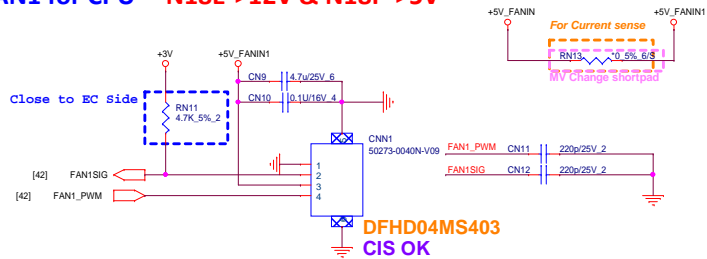


PROJECT : Valkyrie
Quanta Computer Inc.

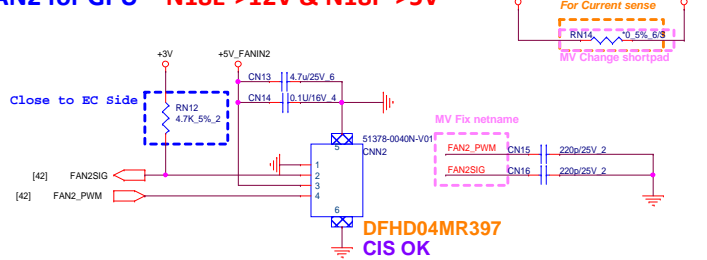
Size B	Document Number EMI/RF Solution/HOLE	Rev 1A
Date: Tuesday, April 07, 2020	Sheet 37 of 106	



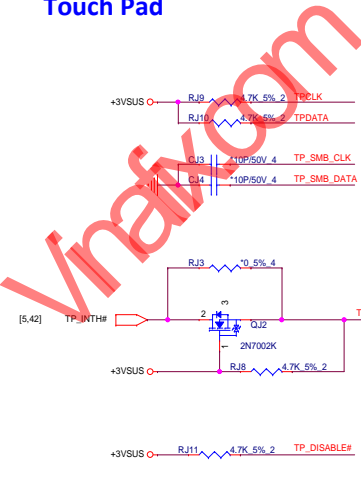
FAN1 for CPU N18E->12V & N18P->5V



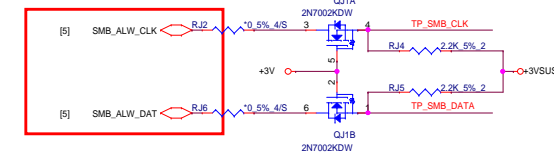
FAN2 for GPU N18E->12V & N18P->5V



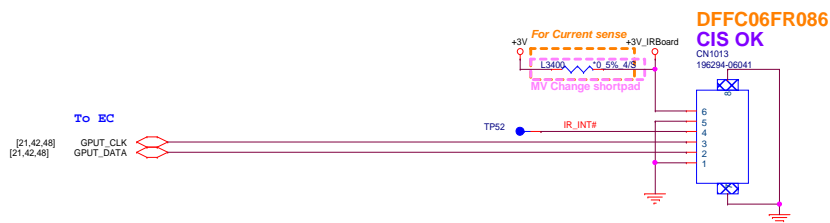
Touch Pad



BIOS change to I2C



IR connector



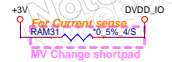
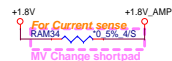
For Debug Card



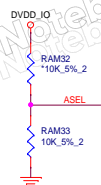
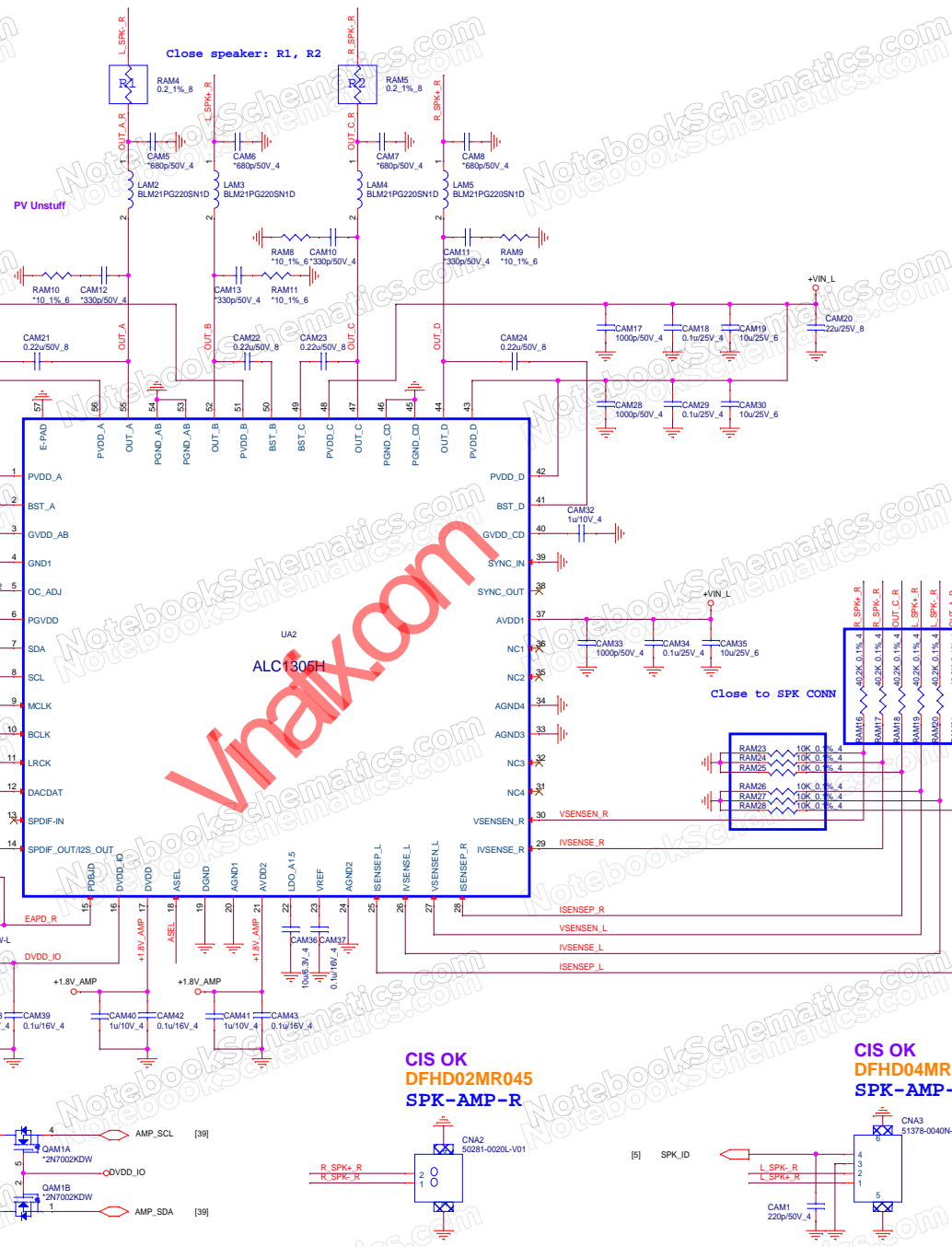
20mil

20mil

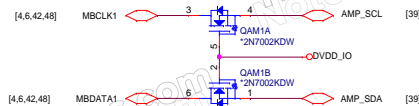
30mil



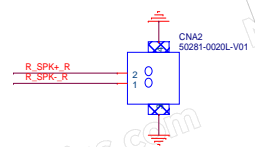
Power domain:
PVDD: 6-26V
DVDD & AVDD2: 1.8V
DVDD_IO: 1.8V-3.3V (default: 3.3V)



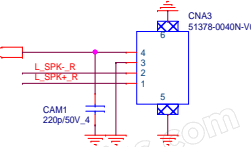
I2C Address
Select n
Low0 x20
Hi: 0x22



CIS OK
DFHD02MR045
SPK-AMP-R

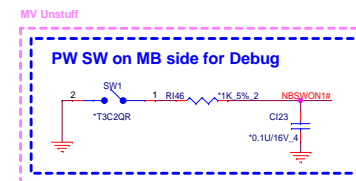


CIS OK
DFHD04MR397
SPK-AMP-L

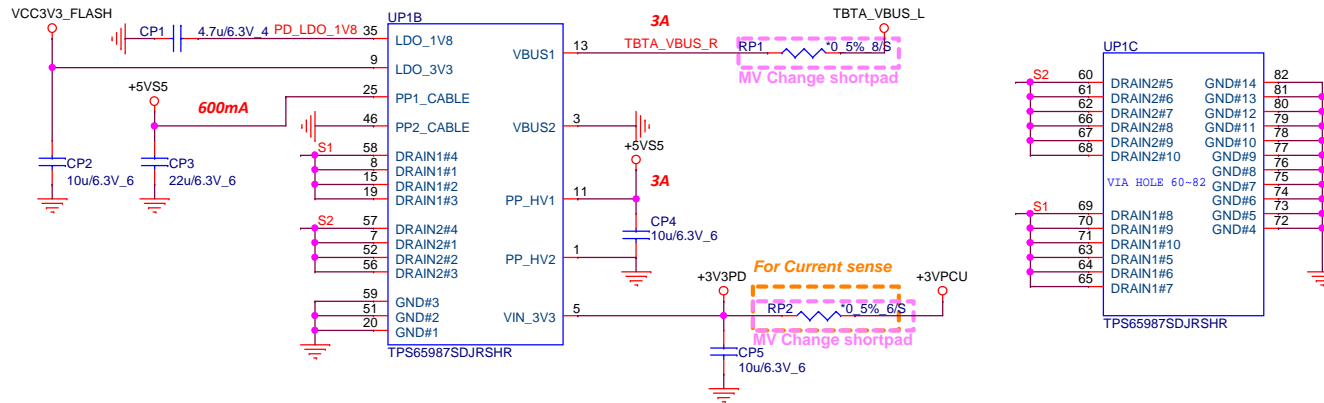


PROJECT : Valkyrie
Quanta Computer Inc.

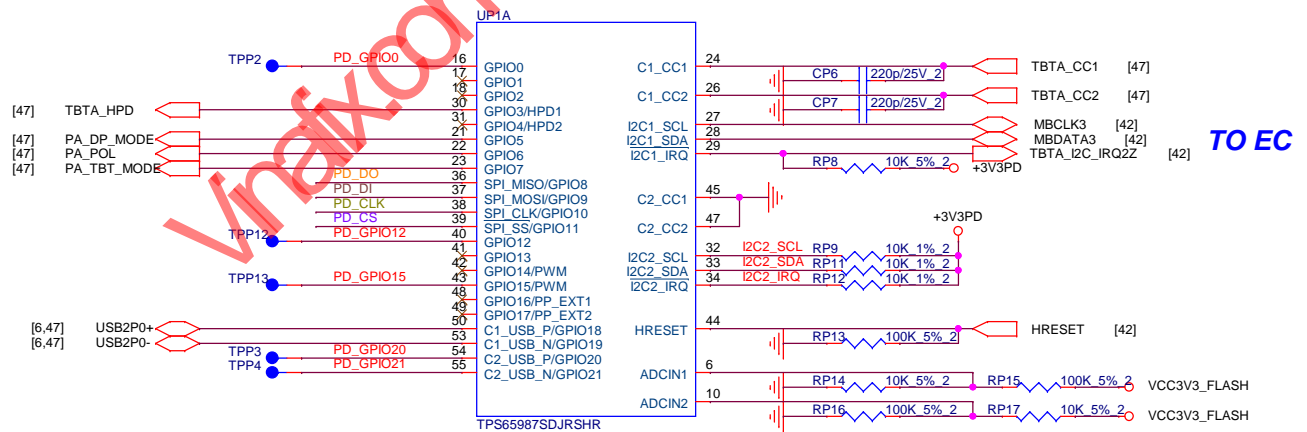
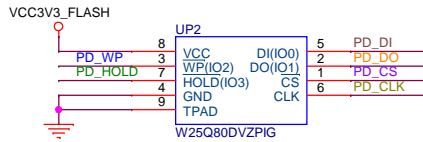
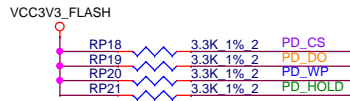
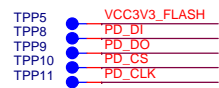
Size C Document Number
Speaker AMP ALC1305H-CG
Rev 1A
Date: Tuesday, April 07, 2020 Sheet 1 of 106



PD TPS65987DDJRSHR



PD SPI ROM

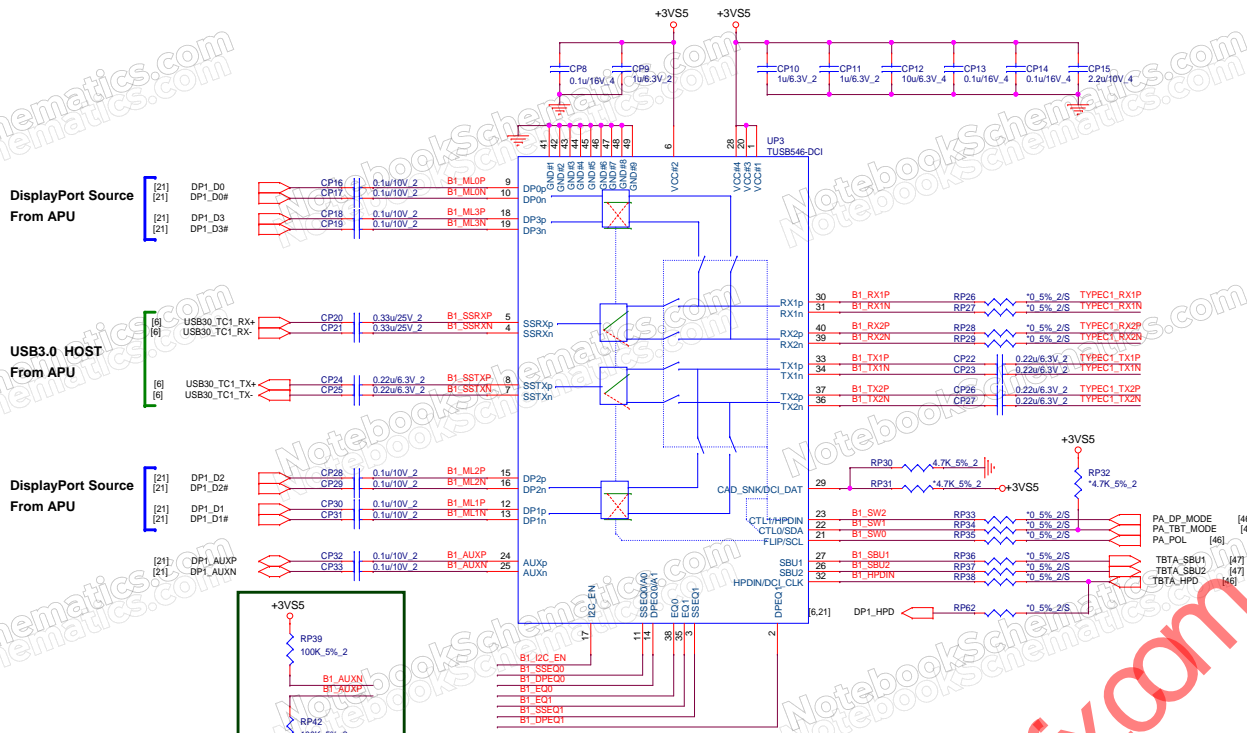


Qunata PN	Part Description
AL180901000	IC OTHER(56P) SN1809018RSHR(VQFN)



PROJECT : Valkyrie
Quanta Computer Inc.

Size B	Document Number	Rev 1A
	PD TPS65987DDJRSHR	
Date: Tuesday, April 07, 2020	Sheet 46 of 106	



TI: RP39/42 need to be placed

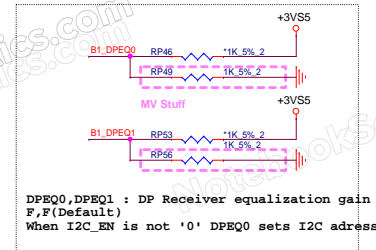
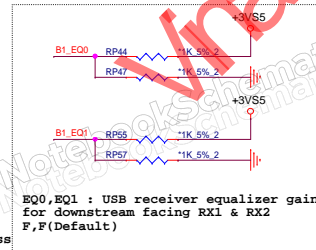
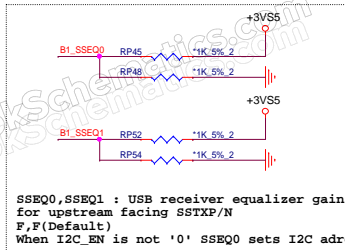
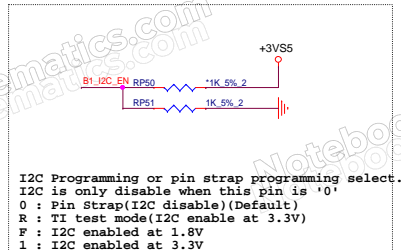


Table 7. TUSB546-DCI Receiver Equalization GPIO Control

Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS			USB 3.1 UPSTREAM FACING PORT			ALL DISPLAYPORT LANES		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	SSEQ0 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	0.2	0	0	-1.6	0	0	-1.6
1	0	R	1.2	0	R	-0.5	0	R	-3.3
2	0	F	2.2	0	F	0.5	0	F	4.9
3	0	1	3.3	0	1	1.6	0	1	6.5
4	R	0	4.2	R	0	2.4	R	0	7.5
5	R	R	5.1	R	R	3.4	R	R	8.6
6	R	F	5.9	R	F	4.1	R	F	9.5
7	R	1	6.7	R	1	4.9	R	1	10.4
8	F	0	7.4	F	0	5.7	F	0	11.1
9	F	R	8.1	F	R	6.4	F	R	11.7
10	F	F	8.7	F	F	6.9	F	F	12.3
11	F	1	9.3	F	1	7.5	F	1	12.8
12	1	0	9.7	1	0	8.0	1	0	13.2
13	1	R	10.2	1	R	8.5	1	R	13.6
14	1	F	10.6	1	F	8.9	1	F	14.0
15	1	1	11.1	1	1	9.4	1	1	14.4

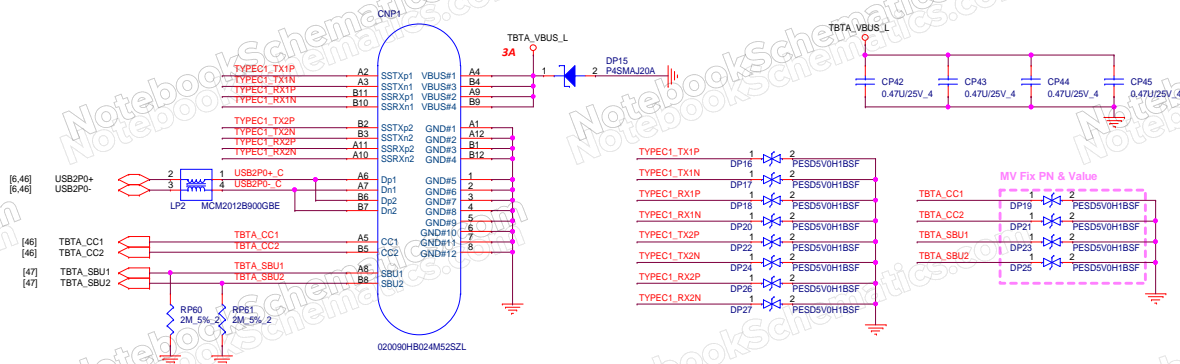
USB546 Pin Control Mode

CTL1	CTL0	FLIP	TUSB546 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

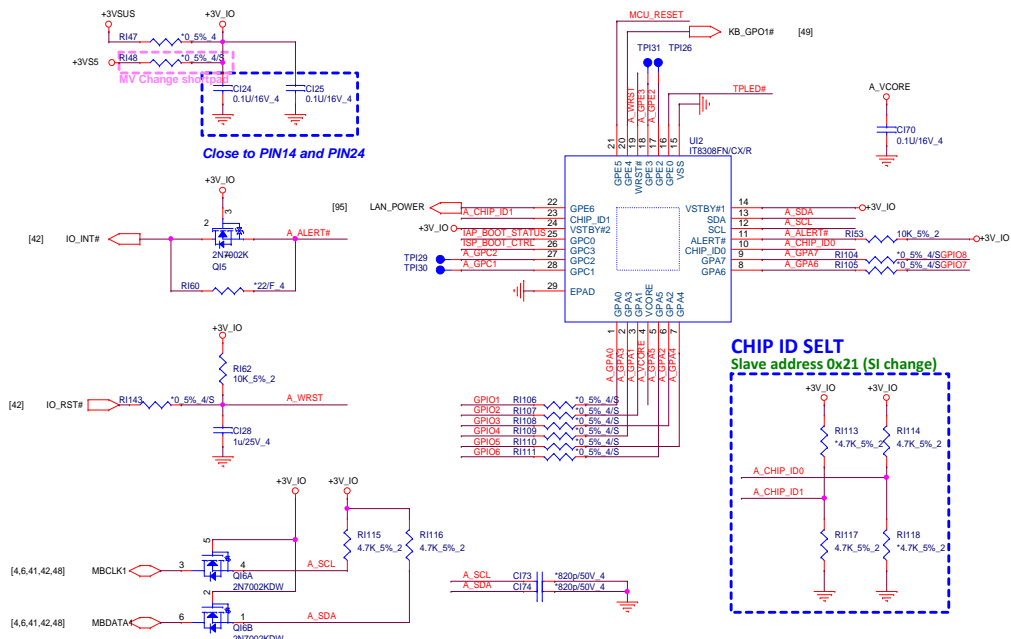
AUX Pin Control Mode

CTL1	FLIP	AUX Select
H	L	AUXP->SBU1, AUXN->SBU2
H	H	AUXP->SBU2, AUXN->SBU1
L>2ms	X	Open

4 Level Input:
L: Option1 Tie 1Kohm 5% to GND
Option2 Directly tie to GND
R: Tie 20kohm 5% to GND
F: Float(leave pin open)
1: Option1 Tie 1Kohm 5% to Vcc
Option2 Directly tie to Vcc

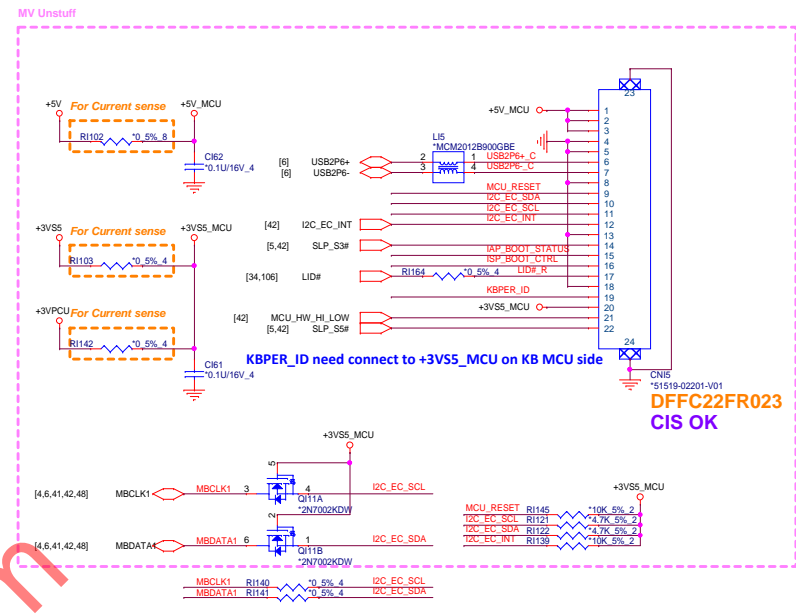
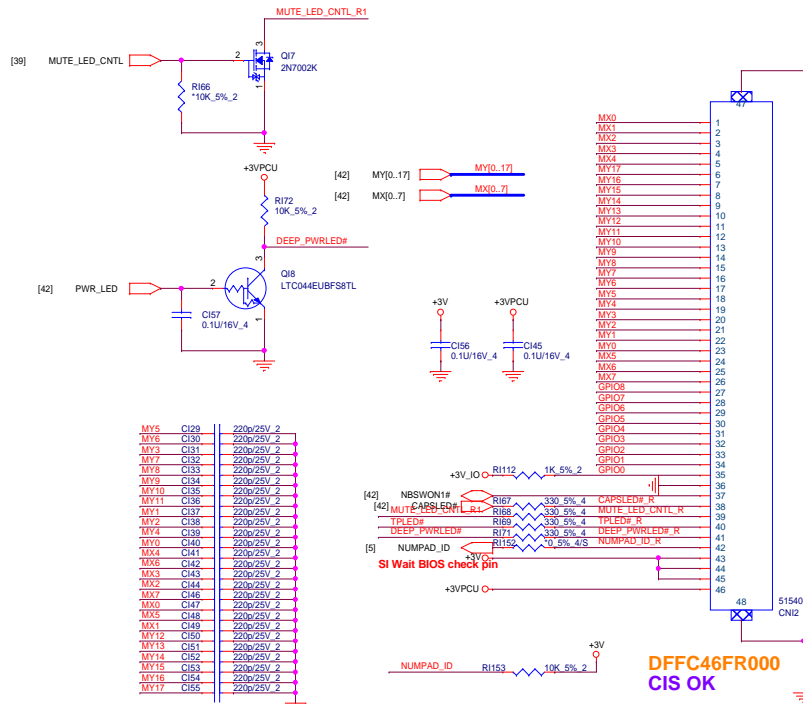


GPIO EXPENDER

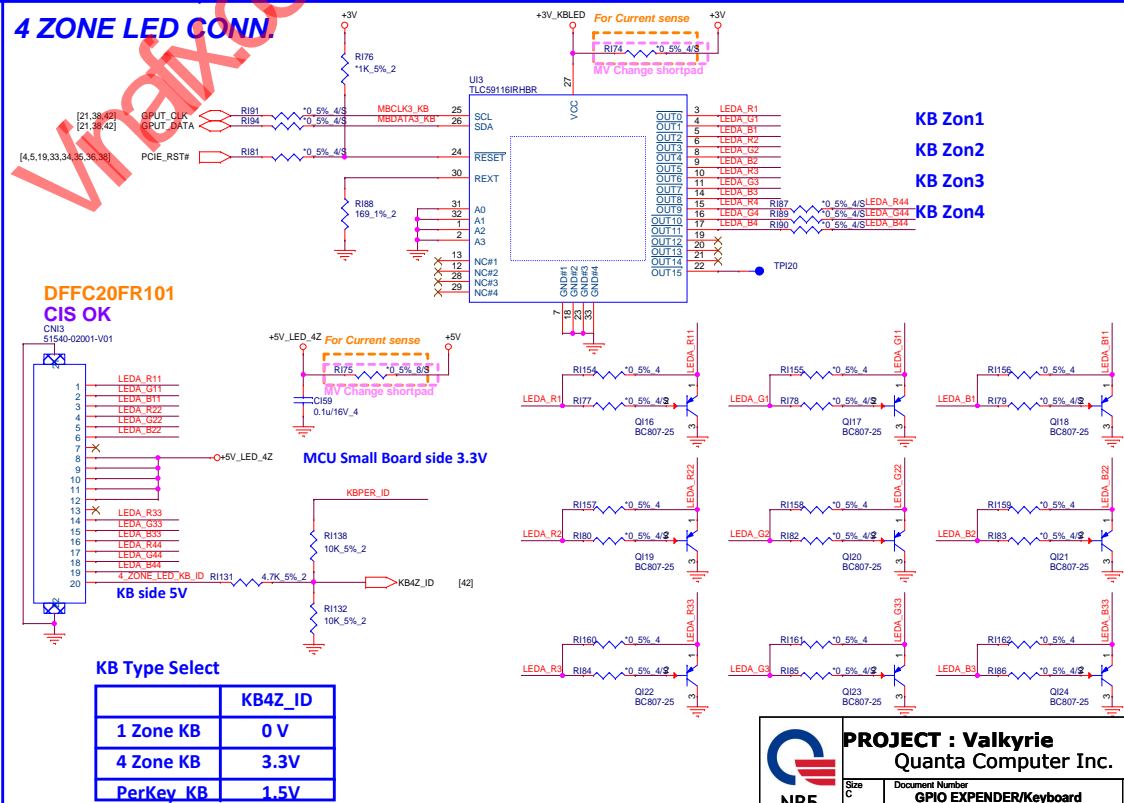


Per Key to MCU Board

48

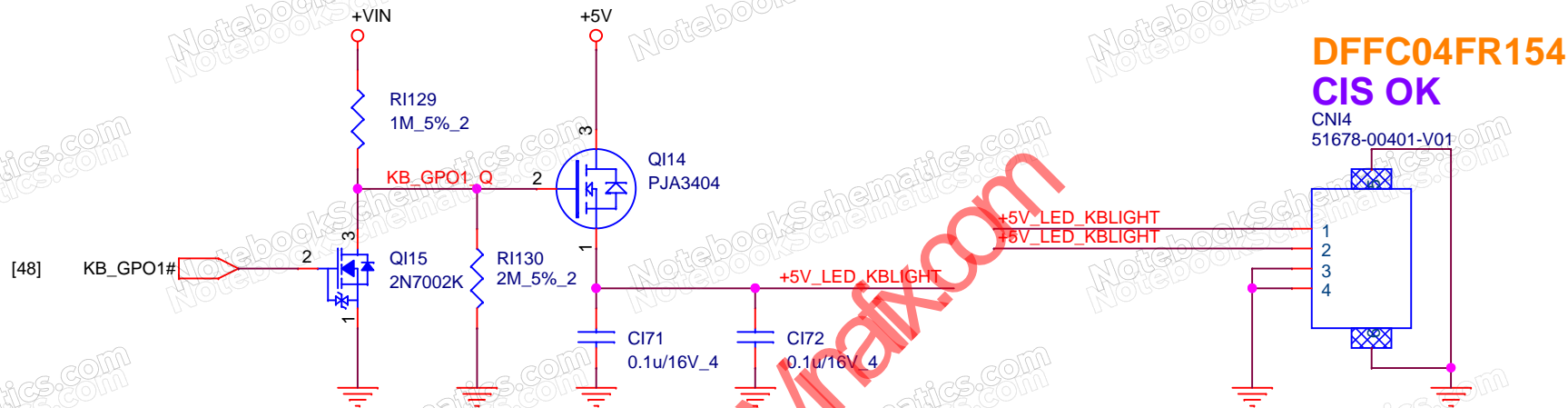
**KEYBOARD CONN.**


4 ZONE LED CONN.



1 zone LED KEYBOARD BACKLIGHT CONN.

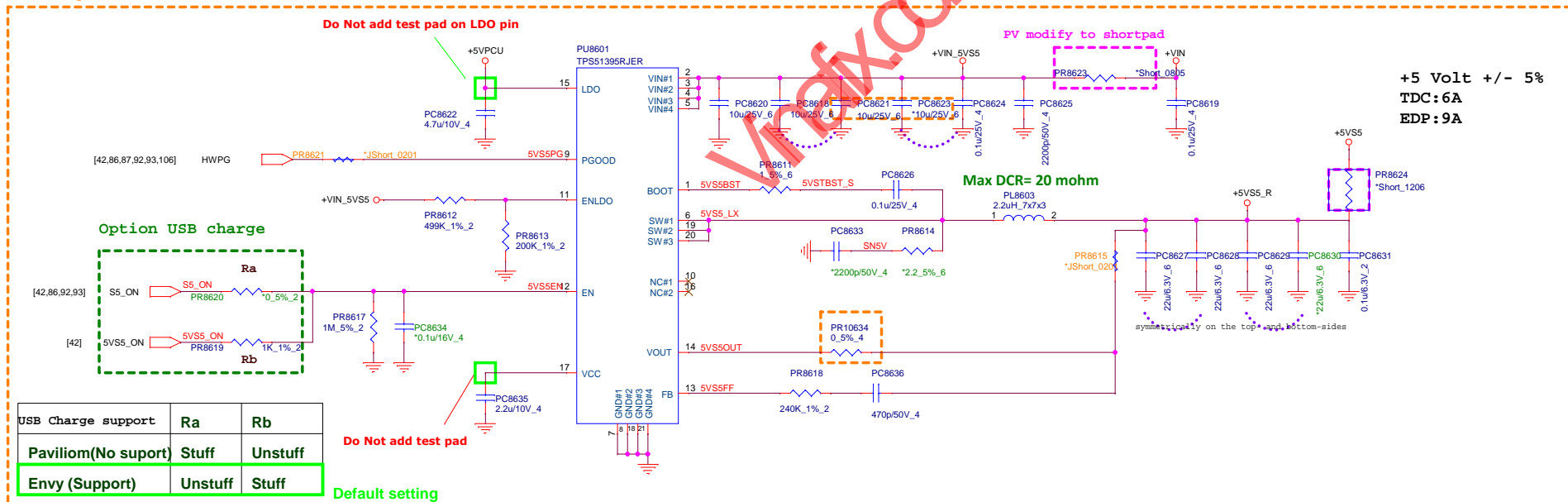
49



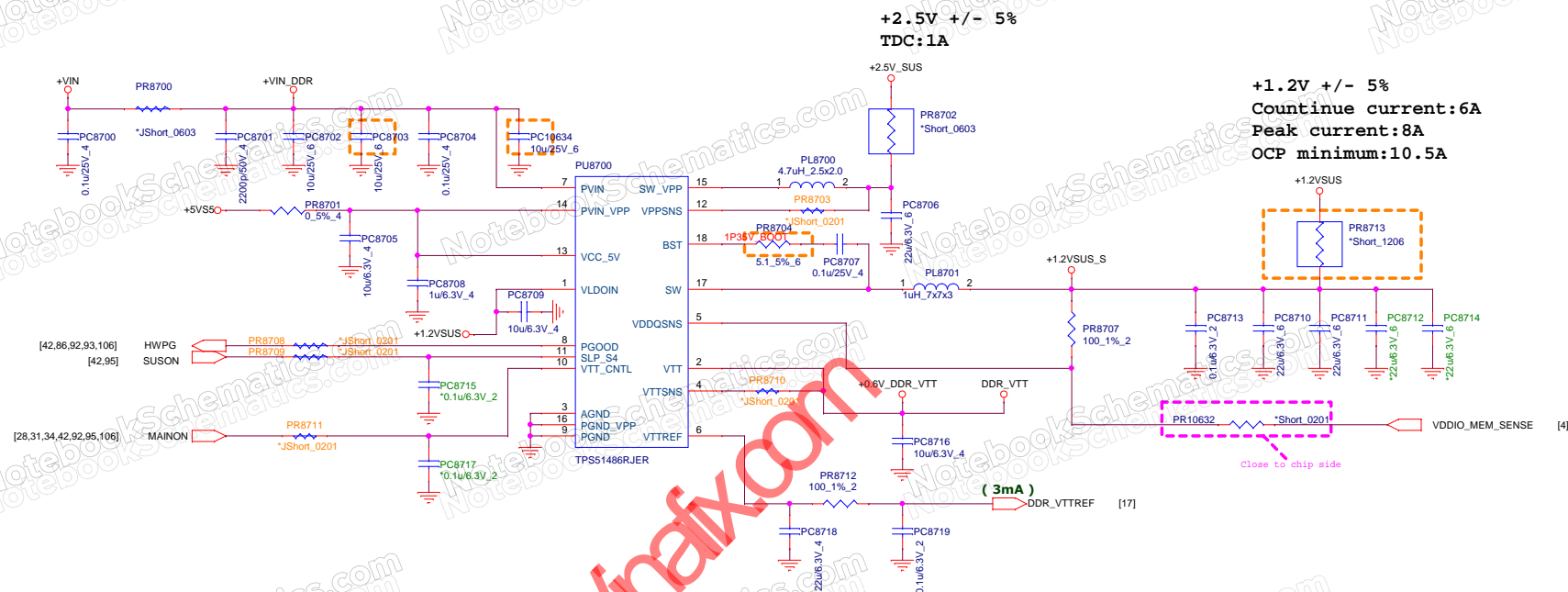
 NB5	PROJECT : Valkyrie Quanta Computer Inc.		
	Size A	Document Number 1 Zone LED	Rev 1A
	Date: Tuesday, April 07, 2020		Sheet 49 of 106

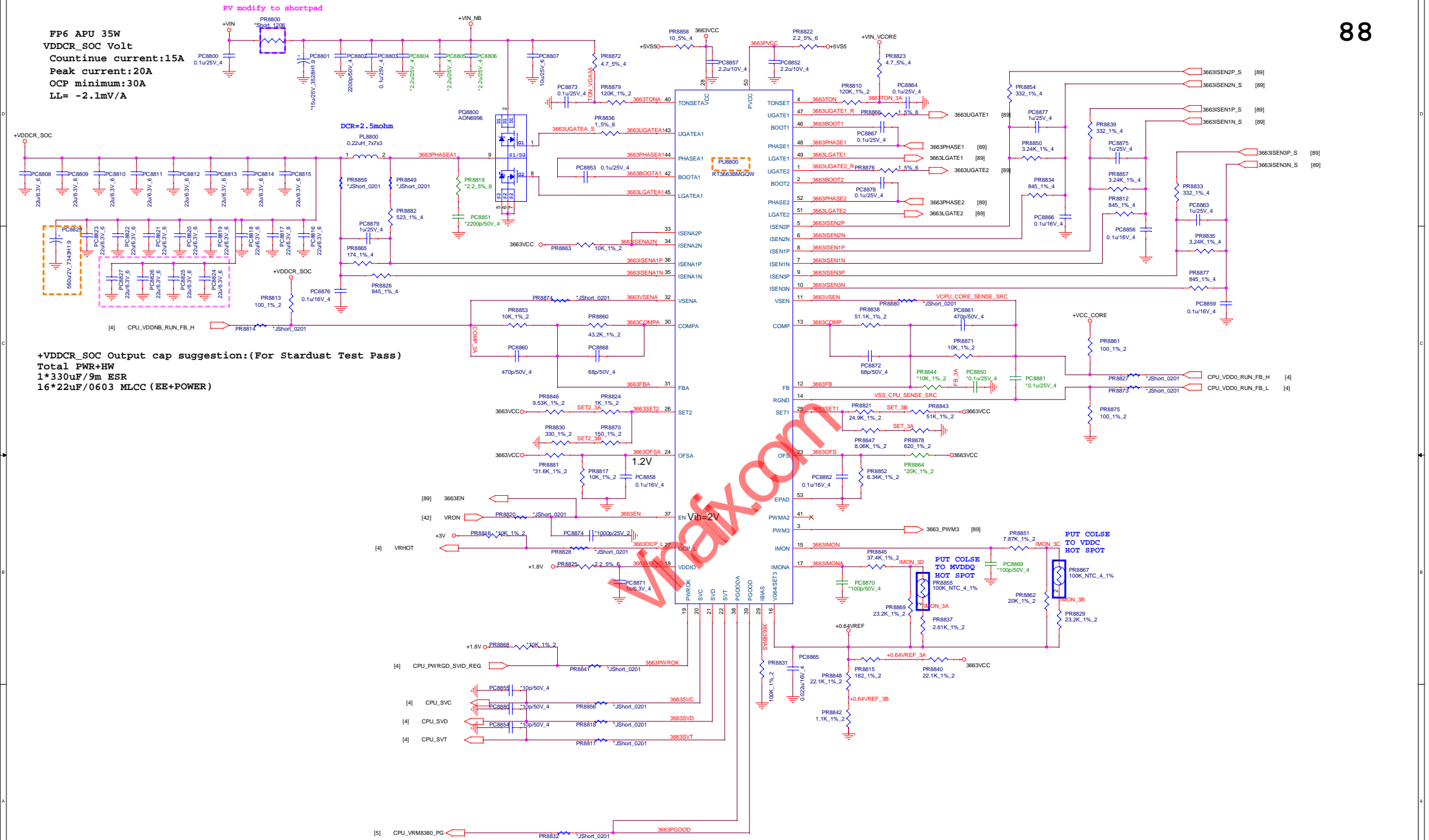


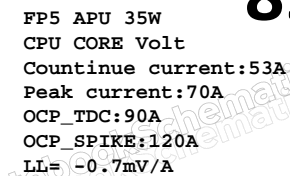
Size	Document Number	Rev
	Charge	1A
Date:	Tuesday, April 07, 2020	Sheet 82 of 106



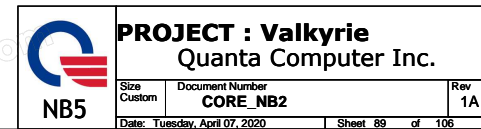
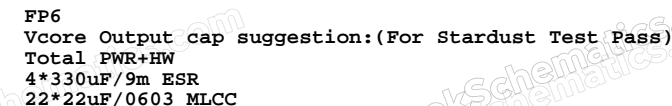
USB Charge support	Ra	Rb
Paviliom(No suport)	Stuff	Unstuff
Envy (Support)	Unstuff	Stuff

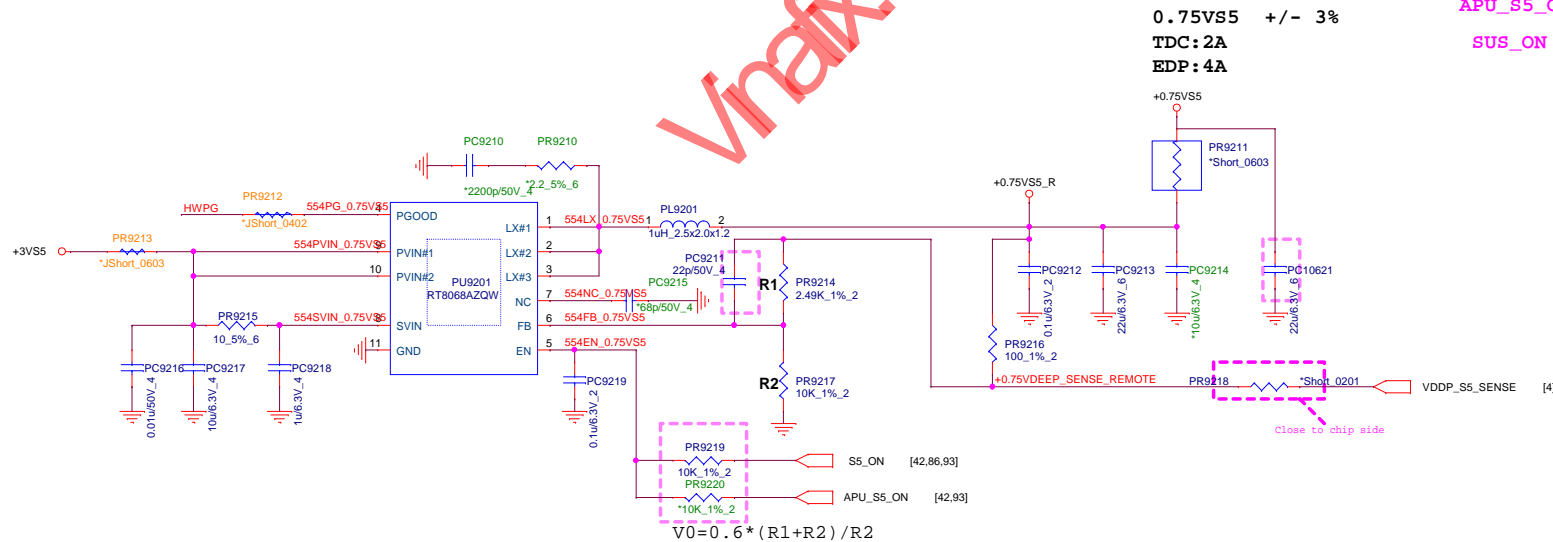
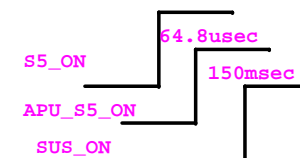
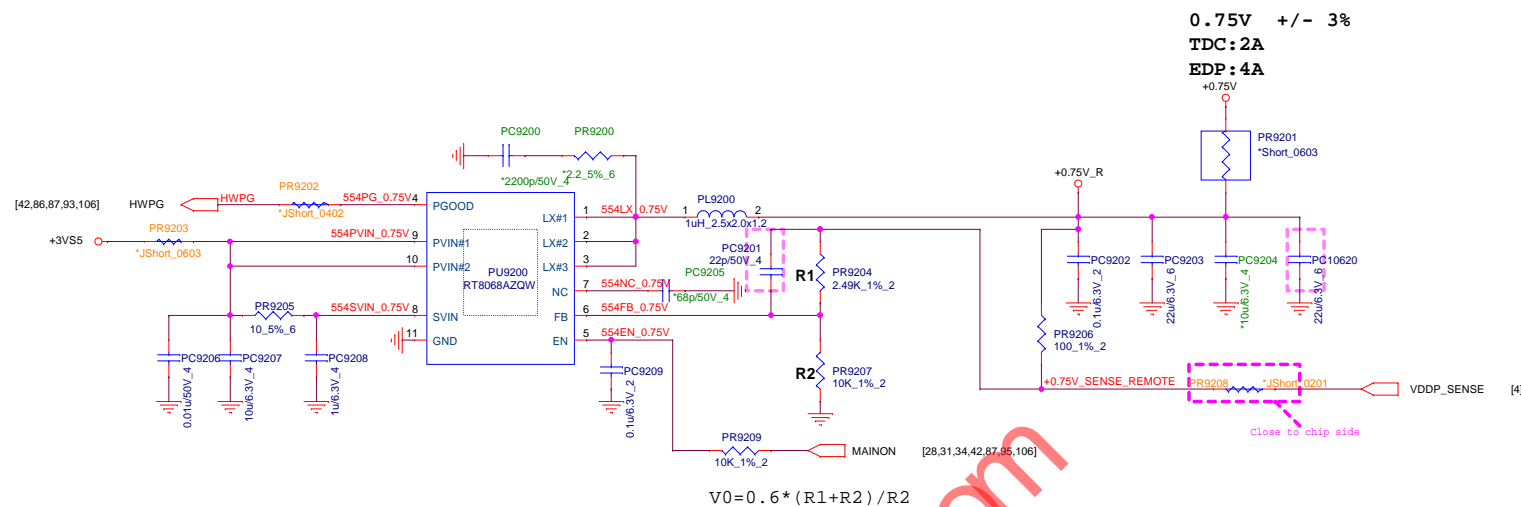






FP6 APU 35W
CPU CORE Volt
Countinue current:51A
Peak current:90A
OCP_TDC:110A
OCP_SPIKE:145A
LL= -0.7mV/A





[41,49,82,86,87,88,89,95,97,101,106]

+VIN

[4,5,6,7,19,22,34,38,95,105]

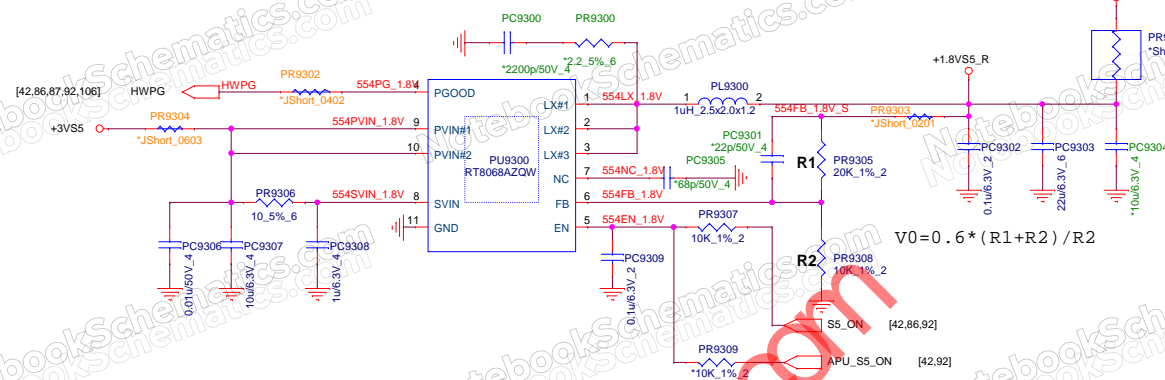
+1.8VS5

1.8VS5 +/- 3%

TDC: 3A

EDP: 4A

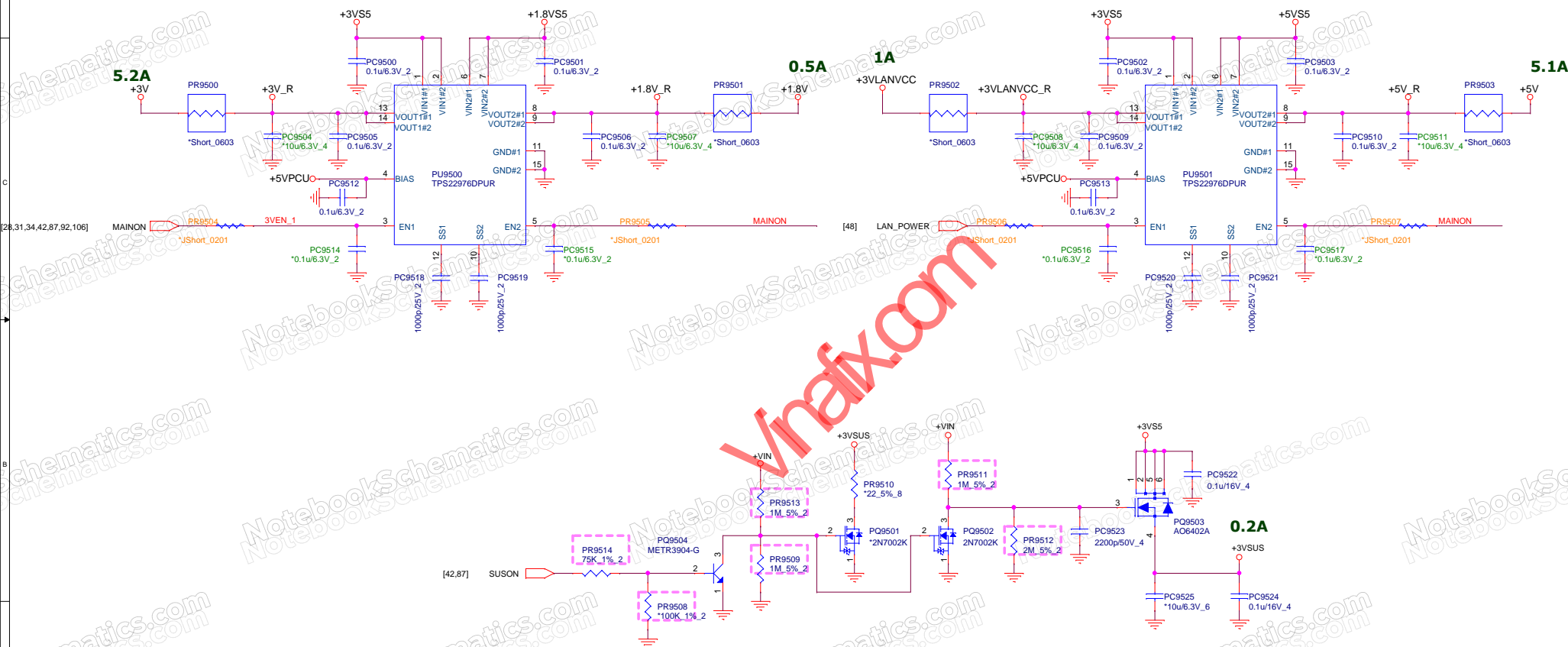
+1.8VS5



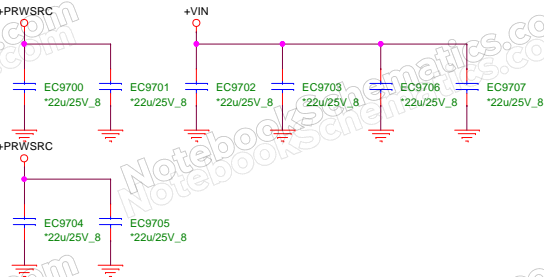
PROJECT : Valkyrie
Quanta Computer Inc.

Size Custom	Document Number +0.95V(AOZ2260/+1.8VS5)	Rev 1A
Date: Tuesday, April 07, 2020	Sheet 93	of 106

+3V	[4,5,7,17,18,21,27,28,30,31,33,34,35,36,38,39,41,42,48,82,88,98,99,101,105]
+5VS5	[34,46,86,87,88,89,98,101,105]
+3VS5	[4,5,6,7,23,31,35,36,42,47,48,82,86,92,93,104,105,106]
+3VSUS	[38,48]
+5V	[28,30,39,48,49,104,106]
+3VLAVCC	[33]
+5VPCU	[39,82,86,105]



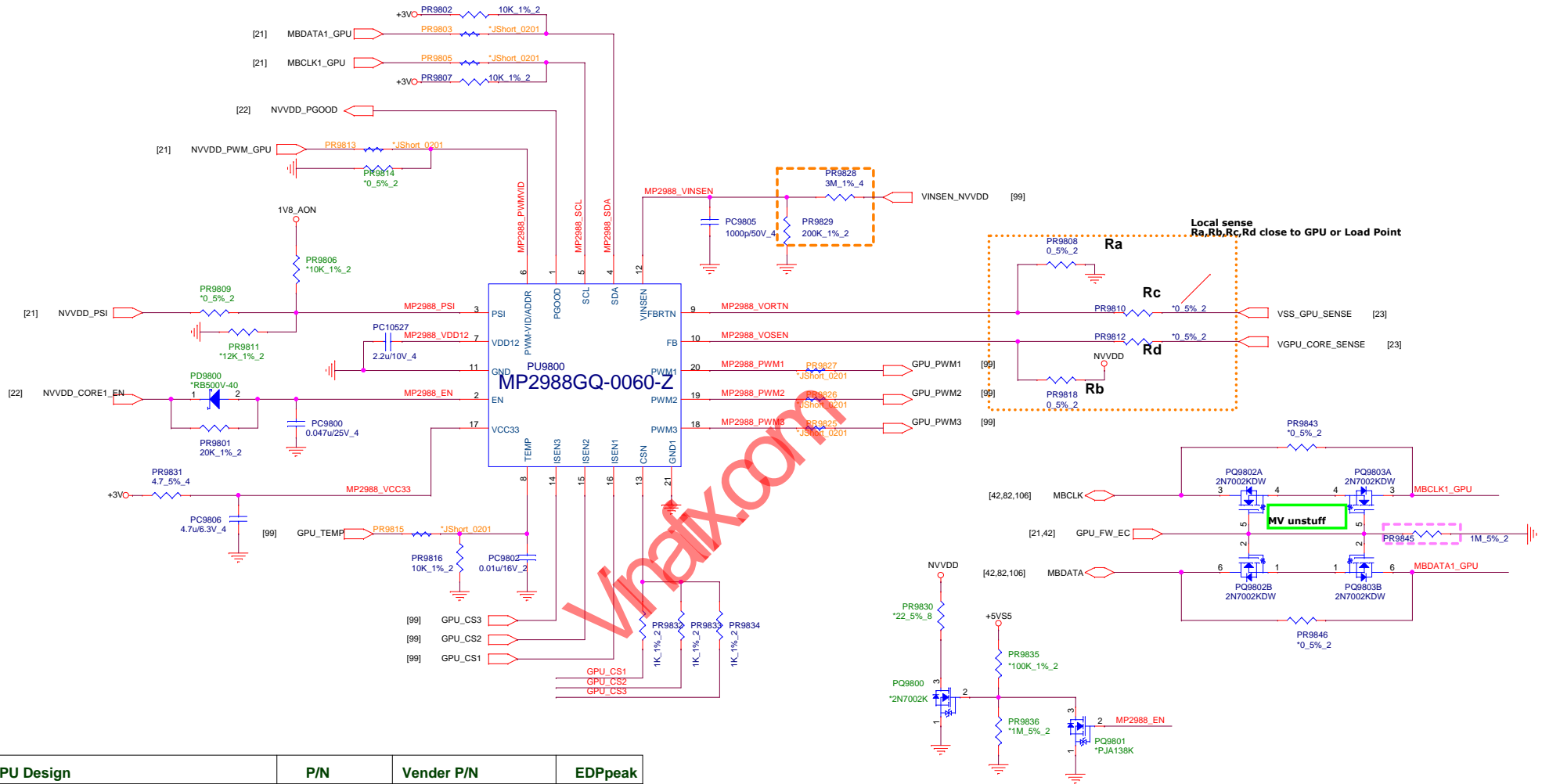
Reserve for ISEN



Vinafx.com

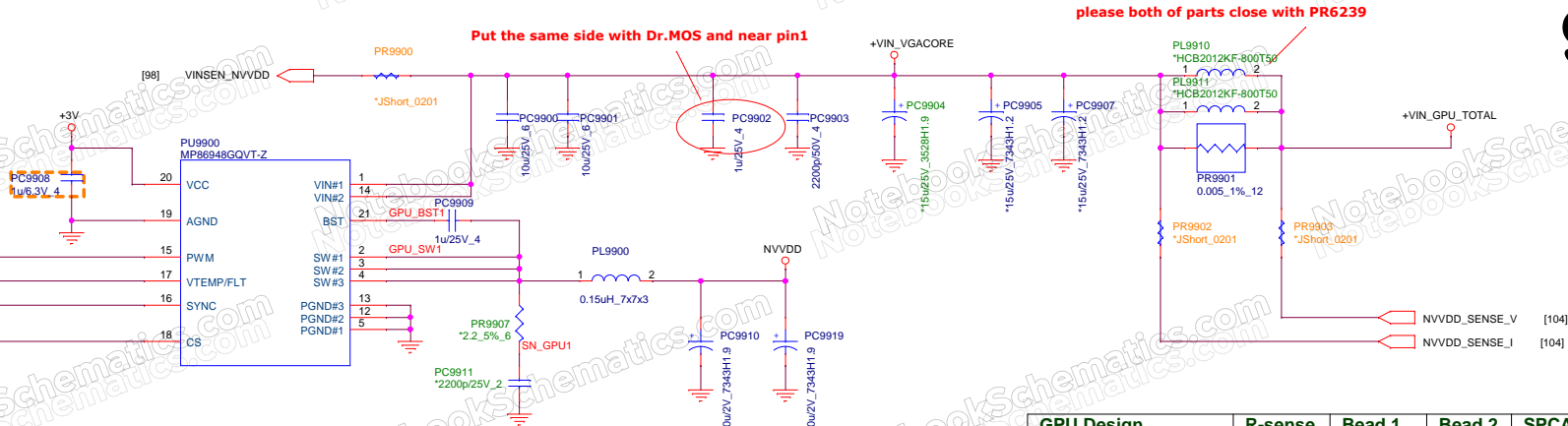
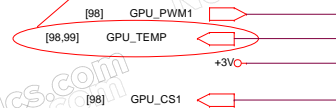


PROJECT : Valkyrie Quanta Computer Inc.		
Size Custom	Document Number 97 – ISN and EMI	Rev 1A
Date: Tuesday, April 07, 2020		
Sheet 97 of 106		

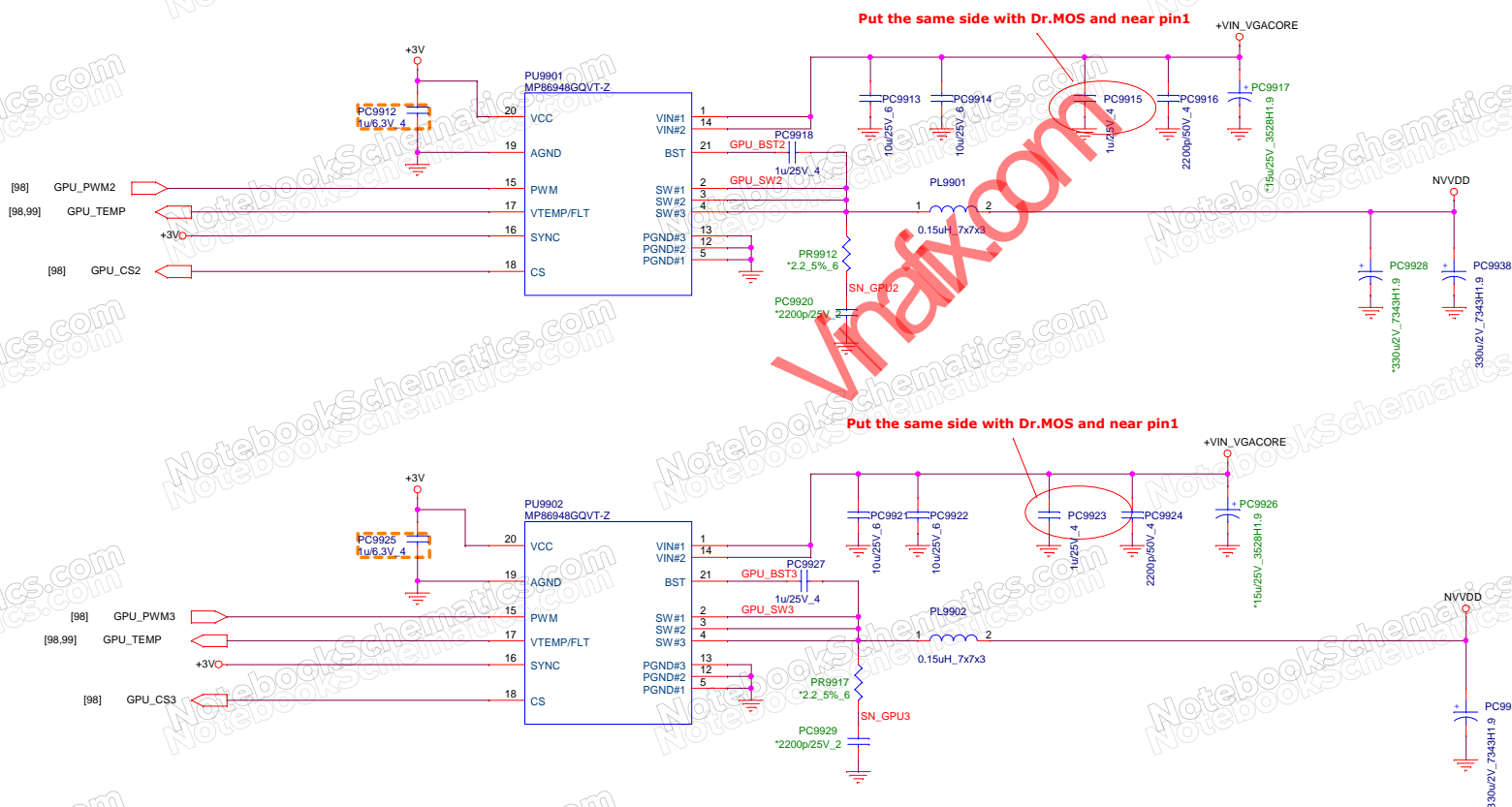


GPU Design	P/N	Vender P/N	EDPpeak
3 Phase for N18P -G0 MAX P (50W/47A)	AL002988000	MP2988GQ-0060-Z	109A
4 Phase for N17P-G1 (50W/59A)	AL002884003	MP2884AGU-0103-Z	106A
5 Phase for N18E -G0 MAXQ (60W/63A)	AL002886005	MP2886AGU-0125-Z	225A
6 Phase for N18E -G3 (80W/84A)	AL002886000	MP2886AGU-0112-Z	300A

+5VS5 [34,46,86,87,88,89,95,101,105]
 1V8_AON [19,21,22,23,24,25,101,105]
 NVVDD [22,23,99]
 +3V [4,5,7,17,18,21,27,28,30,31,33,34,35,36,38,39,41,42,48,82,88]



GPU Design N18P-G0	R-sense Stuff	Bead 1 Unstuff	Bead 2 Unstuff	SPCAR 4pcs
-----------------------	------------------	-------------------	-------------------	---------------

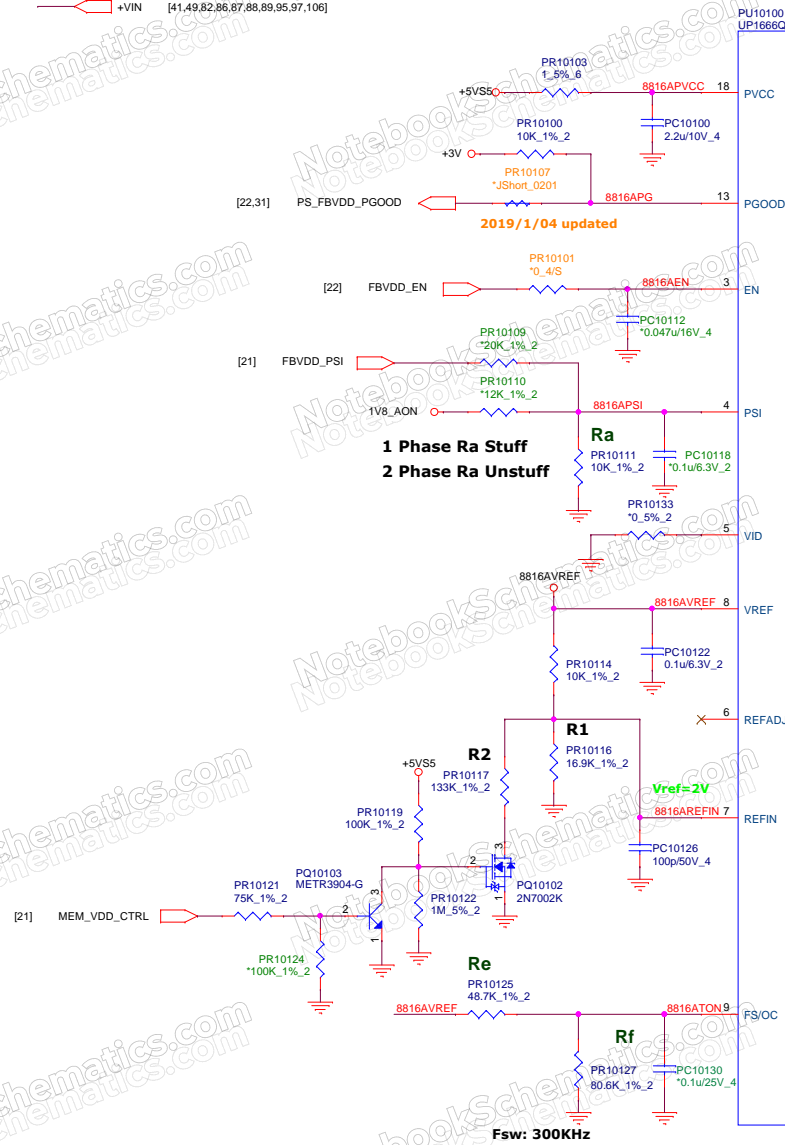


Default setting

```
N18P G0 MP
GPU CORE Volt
Cintinue current:47A
Peak current: 109A/6uSec.
OCP Minimum: 130A.
LL=
VBOOT=0.8V
Eff > 86%
DC < +/- 20mV
Setting time <100uS
```

```
N18P G62
GPU CORE Volt
Cintinue current:45.8A
Peak current: 120.5A/6uSec
OCP Minimum: 130A.
LL=
VBOOT=0.8V
Eff > 86%
DC < +/- 20mV
Setting time <100us
```

+5VS5 [34,46,86,87,88,89,95,98,105]
 NVVDD [22,23,98,99]
 +VIN_GPU_TOTAL [99]
 1V8_AON [19,21,22,23,24,25,98,105]
 FBVDDQ_MEM [20,22,23,24,25]
 +VIN [41,49,82,86,87,88,89,95,97,106]

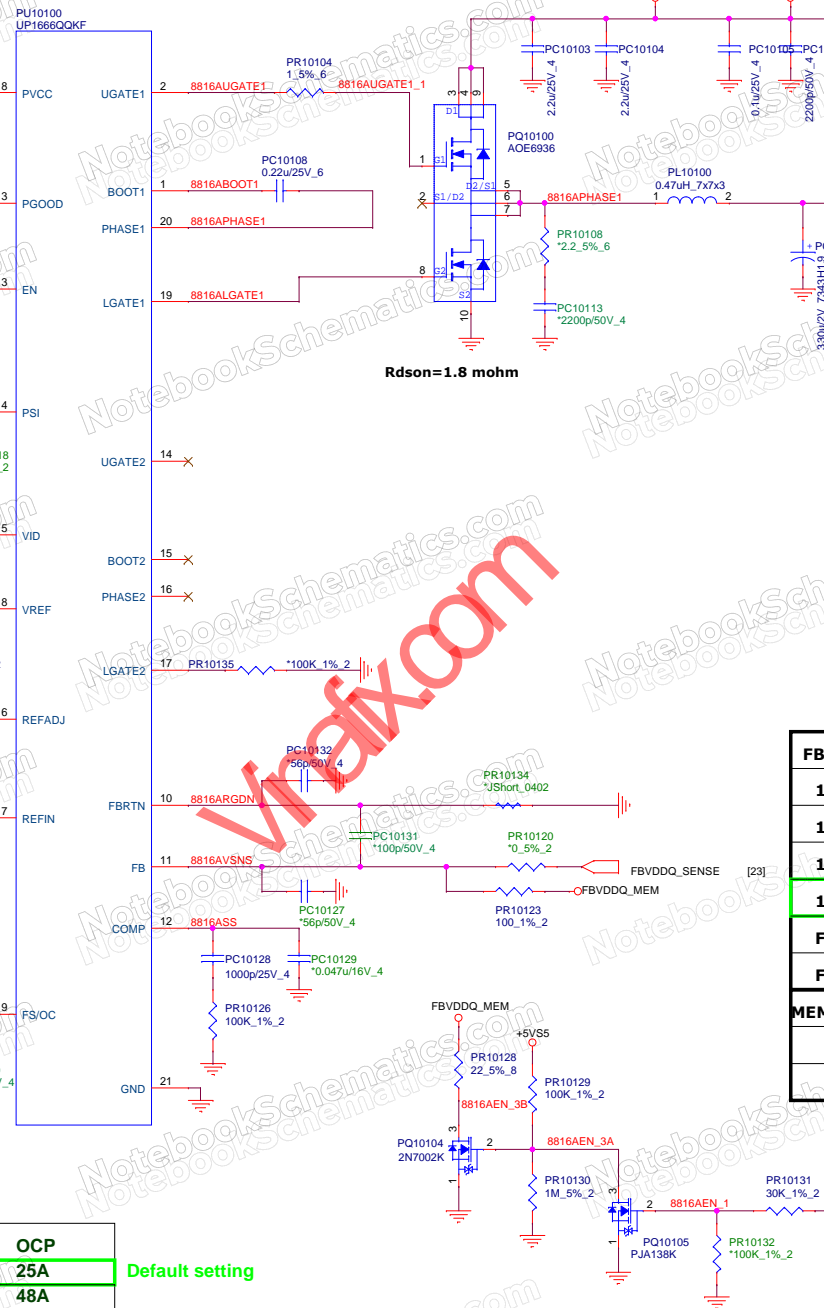


1 Phase Ra Stuff
 2 Phase Ra Unstuff

Fsw = 300KHz

	Ra	Re	Rf	OCP
N18P G0 1-Phase	Stuff	48.7K	80.6K	25A
N18E G0 2-Phase	Unstuff			48A

Default setting



Rdson=1.8 mohm

GPU Design	R-sense	VIN bead	SPCAP
N18P-G0	Stuff	Unstuff	2pcs

FBVDDQ_MEM	R1	R2	GPU Type
1.55V-1.35V	34.8K	53.6K	
1.5V_1.35V	30.9K	69.8K	N18P_N17P_GDDR5
1.25V_1.35V	21K	80.6K	N18E_GDDR6
1.2V_1.25V	16.9K	133K	N18P_GDDR6
Fix 1.35V	21K	Open	
Fix 1.5V	30.1K	Open	
MEM_VDD_CTRL	FBVDDQ_MEM		
1	1.5V_1.55V		
0	1.35V		

Default setting

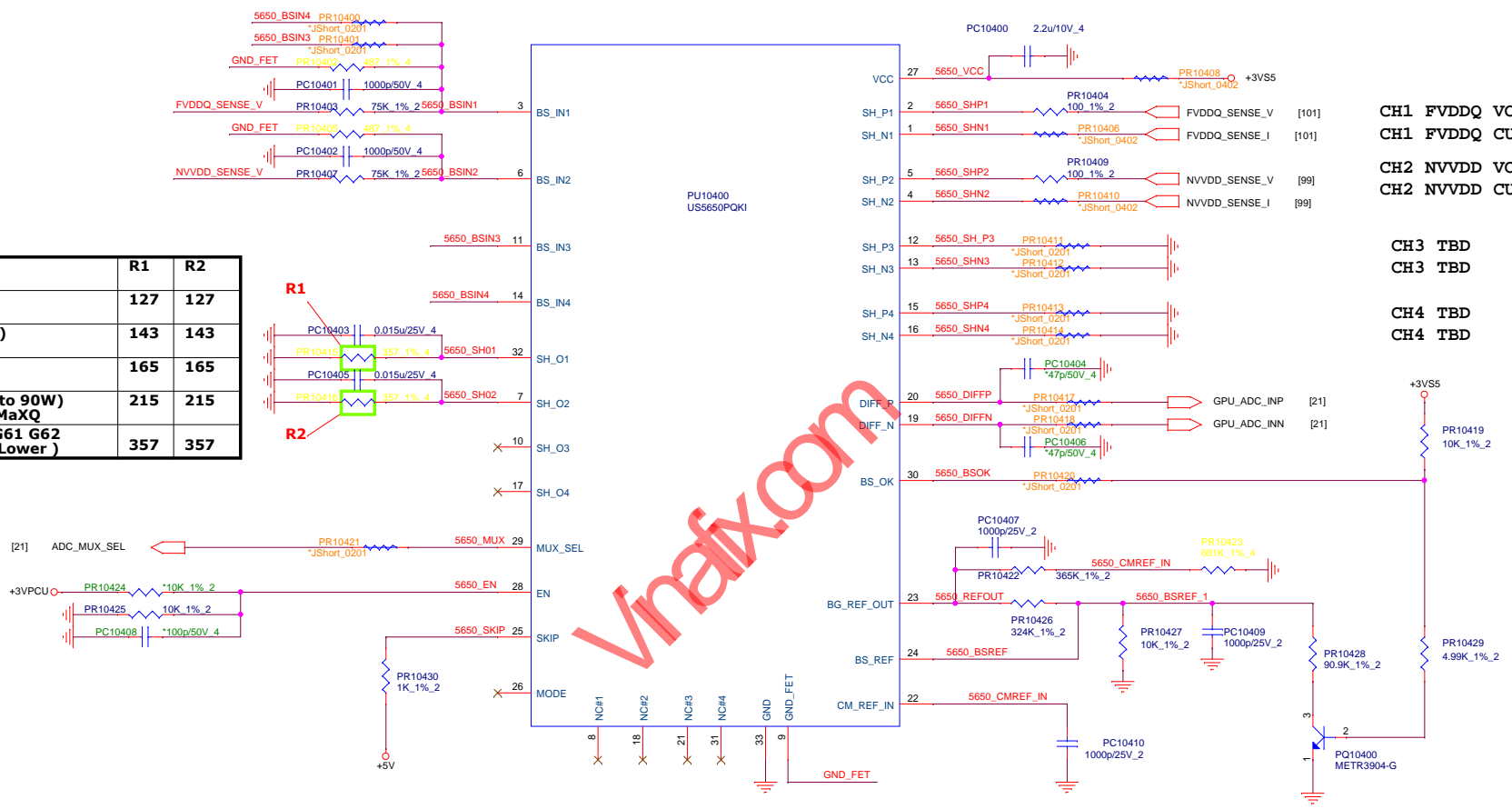
N18P-G0 Max P(50W) +GDDR5
 EDP-C: 14A
 EDP-P: 15A
 OCP minimum: 24A

Default setting

N18P-G62 50W
 EDP-C: 17.2A
 EDP-P: 18.4A
 OCP minimum: 24A

+3V [4,5,7,17,18,21,27,28,30,31,33,34,35,36,38,39,41,42,48,82,88,95,98,99,101,105]

UPI OVR Setting	R1	R2
N18E G3 (150W+)	127	127
N18E G2 (115W to 130W)	143	143
100W to 110W	165	165
N18E-G0,N18E-G1 (75W to 90W) N18E-G2 MaxQ,N18E-G3 MaxQ	215	215
N18P G0 N18P G0 MaxQ G61 G62 N18E G0 MaxQ (70W or Lower)	357	357



CH1 FVDDQ VOLTAGE
CH1 FVDDQ CURRENT
CH2 NVVDD VOLTAGE
CH2 NVVDD CURRENT
CH3 TBD
CH3 TBD
CH4 TBD
CH4 TBD

